



High Speed Super Low Power SRAM

128K Word x 8 Bit

CS18LV11253

Cover Sheet and Revision Status

版別 (Rev.)	DCC No.	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20160063	Jul. 12, 2016	New issue	Hank Lin
2.0	20170013	Jun. 22, 2017	Revise 32L STSOP(I)-8x13.4mm package outline	Hank Lin
3.0	20200019	Dec. 29, 2020	Revise ICC (operating current) 45ns- 20mA, 55ns- 20mA, 70ns- 15mA	Hank Lin



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GENERAL DESCRIPTION

The CS18LV11253 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 131,072 words by 8bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide high speed, super low power features and maximum access time of 45/55/ 70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable inputs (/CE1, CE2) and active LOW output enable (/OE).

The CS18LV11253 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV11253 is available in JEDEC standard 32-pin STSOP (8x13.4 mm), TSOP (8x20mm), TSOP (II) (400mil), and SOP (450 mil) packages.

FEATURES

- Low operation voltage : 2.7 ~ 3.6V
- Ultra-low power consumption :
 - operating current: 20mA (Max.) @ $t_{AA}=45ns$
 - standby current : 2uA (Typ.)
- High speed access time: 45/55/70ns
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible, fully static operation
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE1, CE2 and /OE options.

Product Family

Part No.	Operating Temp	Standby (Max.) ($V_{CC} = 3.6V$)	V_{CC} Range (V)	Speed (ns)	Package Type
CS18LV11253	0~70°C	8uA	2.7~3.6	45/ 55/ 70	32L SOP
	-40~85°C				32L STSOP 1
					32L TSOP 1
					32L TSOP 2
					Dice

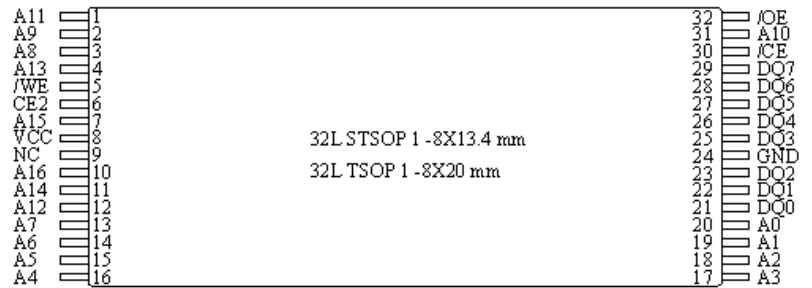
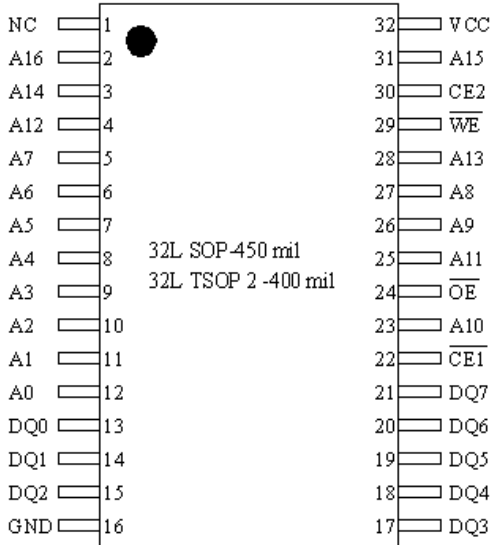


High Speed Super Low Power SRAM

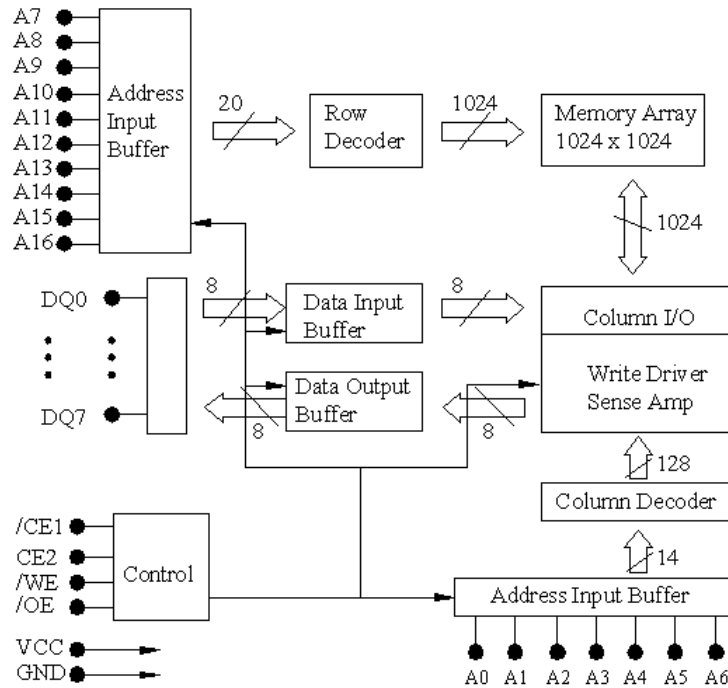
128K Word x 8 Bit

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PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM





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PIN DESCRIPTIONS

Name	Type	Function
A0 – A16	Input	Address inputs for selecting one of the 131,072 x 8 bit words in the RAM
/CE1, CE2	Input	/CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground
NC		No connection

TRUTH TABLE

MODE	/CE1	CE2	/WE	/OE	DQ0~7	Vcc Current
Standby	H	X	X	X	High Z	IccSB, IccSB1
	X	L	X	X		
Output Disable	L	H	H	H	High Z	Icc
Read	L	H	H	L	D _{OUT}	Icc
Write	L	H	L	X	D _{IN}	Icc



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ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Parameter	Rating	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{BIAS}	Temperature Under Bias	-40 to +125	°C
T _{STG}	Storage Temperature	-60 to +150	°C
P _T	Power Dissipation	1.0	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0~70°C	2.7V ~3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

CAPACITANCE ⁽¹⁾ (T_A = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C _{IN}	Input Capacitance	V _{IN} =0V	6	pF
C _{DQ}	Input/output Capacitance	V _{I/O} =0V	8	pF

This parameter is guaranteed and not tested.



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DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$, $V_{CC} = 3.0\text{V}$)

Name	Parameter	Test Condition	MIN	TYP (1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage ⁽³⁾	$V_{CC}=3.0\text{V}$	-0.3		0.8	V
V_{IH}	Guaranteed Input High Voltage ⁽²⁾	$V_{CC}=3.0\text{V}$	2.2		$V_{CC}+0.3$	V
I_{IL}	Input Leakage Current	$V_{CC}=\text{MAX}$, $V_{IN}=0$ to V_{CC}	-1		1	μA
I_{OL}	Output Leakage Current	$V_{CC}=\text{MAX}$, $/\text{CE}1=V_{IH}$, or $\text{CE}2=V_{IL}$, or $/\text{OE}=V_{IH}$, or $/\text{WE}=V_{IL}$ $V_{IO}=0\text{V}$ to V_{CC}	-1		1	μA
V_{OL}	Output Low Voltage	$V_{CC}=\text{MAX}$, $I_{OL}=2.1\text{mA}$			0.4	V
V_{OH}	Output High Voltage	$V_{CC}=\text{MIN}$, $I_{OH} = -1.0\text{mA}$	2.4			V
I_{CC}	Operating Power Supply Current	$F=f_{\text{max}}$, $V_{CC}=V_{CC\text{max}}$, $I_{OUT}=0\text{mA}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	45ns		20	mA
			55ns		20	
			70ns		15	
I_{CCSB}	TTL Standby Supply	$/\text{CE}1=V_{IH}$, $I_{DQ}=0\text{mA}$,			0.4	mA
I_{CCSB1}	CMOS Standby Current	$/\text{CE}1 \geq V_{CC}-0.2\text{V}$, $\text{CE}2=0.2\text{V}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$,		2	8	μA

1. Typical characteristics are at $T_A = 25^\circ\text{C}$.
2. Overshoot: $V_{CC} + 2.0\text{V}$ in case of pulse width $\leq 20\text{ns}$.
3. Undershoot: $- 2.0\text{V}$ in case of pulse width $\leq 20\text{ns}$.
4. Overshoot and undershoot are sampled, not 100% tested.



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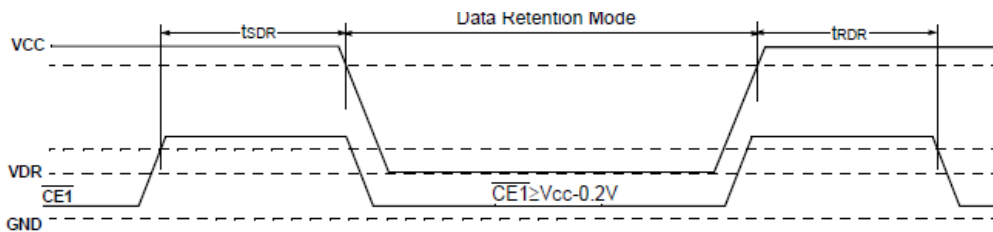
DATA RETENTION CHARACTERISTICS ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$)

Name	Parameter	Test Condition	MIN	TYP ⁽¹⁾	MAX	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CE1} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	1.5			V
I_{CCDR}	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V, V_{CC} = 1.5V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		2	6	μA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (2)			ns

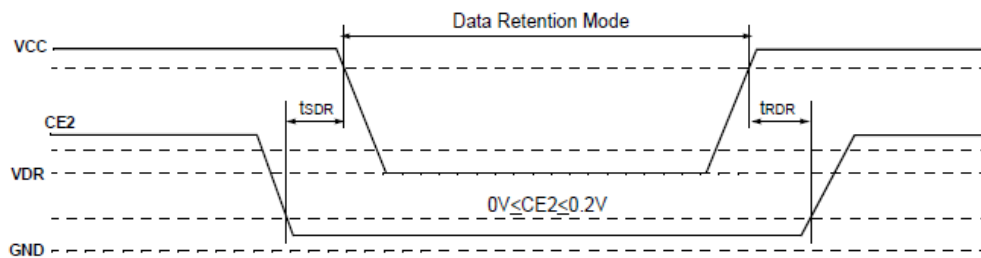
1. $T_A = 25^\circ\text{C}$

1. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CE2$ Controlled)



AC TEST CONDITIONS

Input Pulse Levels	$V_{CC}/0V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Level	$0.5V_{CC}$
Output Load	See Figure 1A and 1B

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC TEST LOADS AND WAVEFORMS

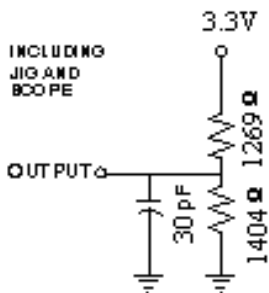


FIGURE 1A

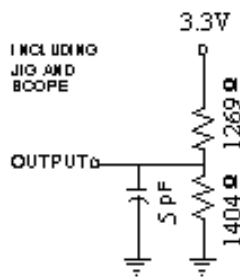


FIGURE 1B

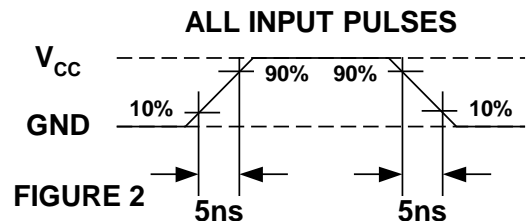


FIGURE 2



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128K Word x 8 Bit

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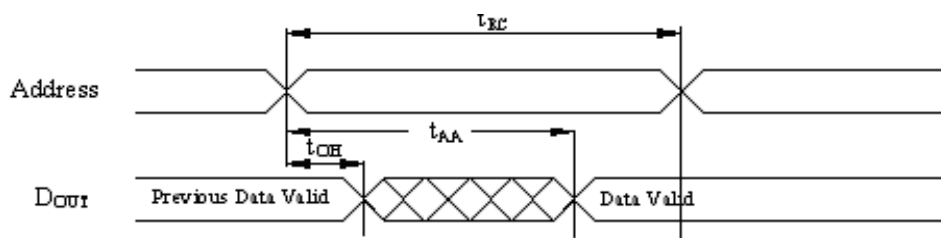
AC ELECTRICAL CHARACTERISTICS (T_A = 0°C ~70°C ; V_{CC}=3.0V)

< READ CYCLE >

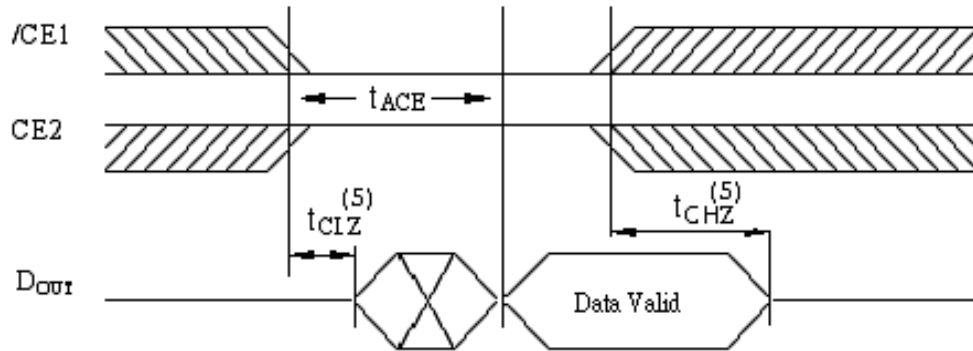
JEDEC Name	Symbol	Description	-45		-55		-70		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{AVAX}	t _{RC}	Read Cycle Time	45		55		70		ns
t _{AVQV}	t _{AA}	Address Access Time		45		55		70	ns
t _{ELQV}	t _{ACE}	Chip Select Access Time		45		55		70	ns
t _{GLQV}	t _{OE}	Output Enable to Output Valid		22		25		35	ns
t _{ELQX}	t _{CLZ} ⁽⁵⁾	Chip Select to Output Low Z	10		10		10		ns
t _{GLQX}	t _{OLZ} ⁽⁵⁾	Output Enable to Output in Low Z	5		5		5		ns
t _{EHQZ}	t _{CHZ} ⁽⁵⁾	Chip Deselect to Output in High Z		18	0	20	0	25	ns
t _{GHQZ}	t _{OHZ} ⁽⁵⁾	Output Disable to Output in High Z		18	0	20	0	25	ns
t _{AXOX}	t _{OH}	Address Change to Out Disable	10		10		10		ns

SWITCHING WAVEFORMS (READ CYCLE)

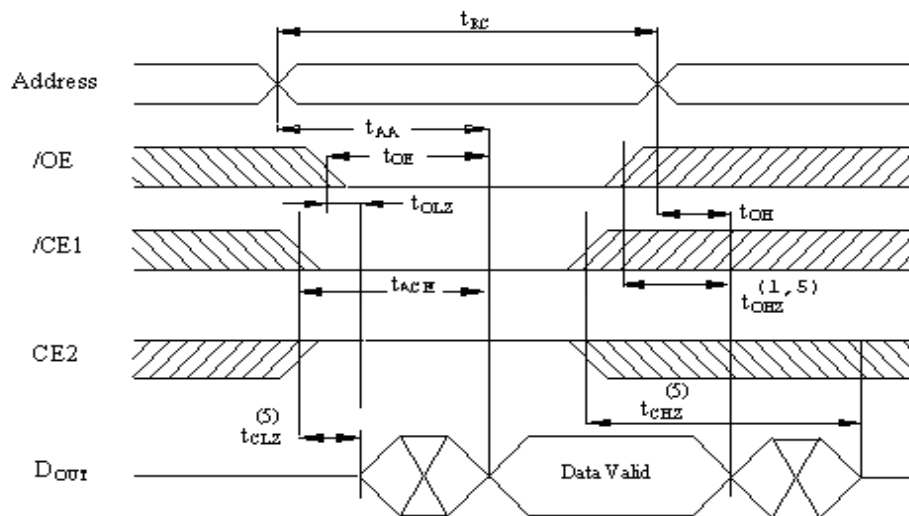
READ CYCLE 1 [1, 2, 4]



READ CYCLE 2 [1, 3, 4]



READ CYCLE 3 [1, 4]



NOTES:

1. \overline{WE} is high in read Cycle.
2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or $CE2$ transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500mV$ from steady state with $CL = 5pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.



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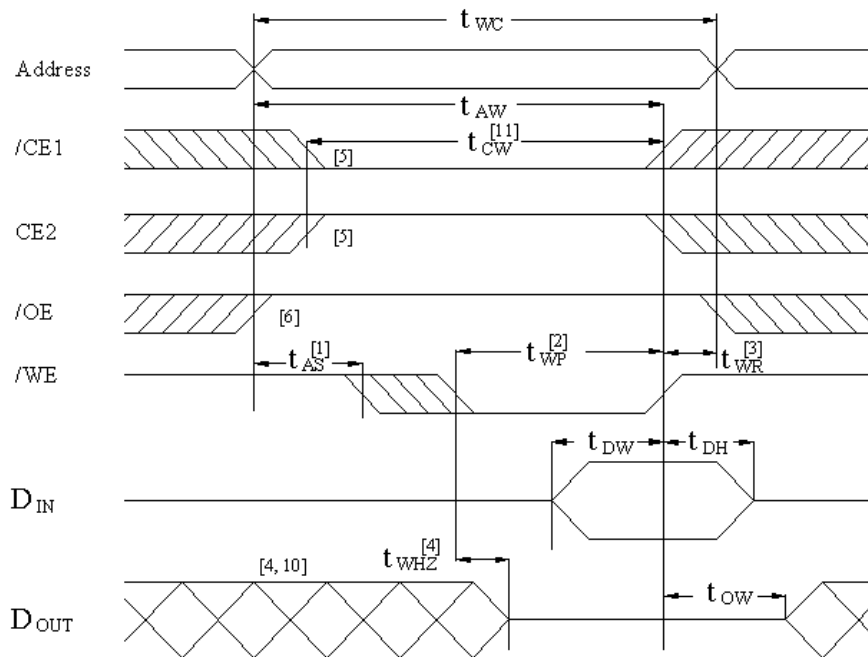
AC ELECTRICAL CHARACTERISTICS (T_A = 0°C ~70°C ; V_{CC}=3.0V)

< WRITE CYCLE >

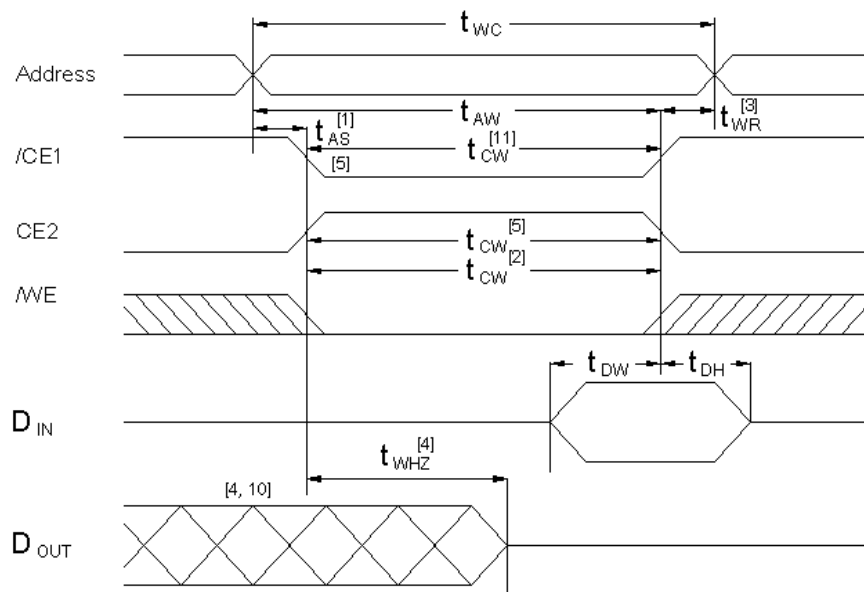
JEDEC Name	Symbol	Description	-45		-55		-70		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{AVAX}	t _{wc}	Write Cycle Time	45		55		70		ns
t _{E1LWH}	t _{cw}	Chip Select to End of Write	35		45		60		ns
t _{AVWL}	t _{as}	Address Setup Time	0		0		0		ns
t _{AVWH}	t _{aw}	Address Valid to End of Write	35		45		60		ns
t _{WLWH}	t _{wp}	Write Pulse Width	35		40		50		ns
t _{WHAX}	t _{wr}	Write Recovery Time	0		0		0		ns
t _{WLQZ}	t _{whz} ⁽¹⁰⁾	Write to Output in High Z		18		20		25	ns
t _{DVWH}	t _{dw}	Data to Write Time Overlap	25		25		30		ns
t _{WHDX}	t _{dh}	Data Hold for Write End	0		0		0		ns
t _{WHOX}	t _{ow} ⁽¹⁰⁾	End of Write to Output Active			5		5		ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



WRITE CYCLE2 (Chip Enable Controlled)





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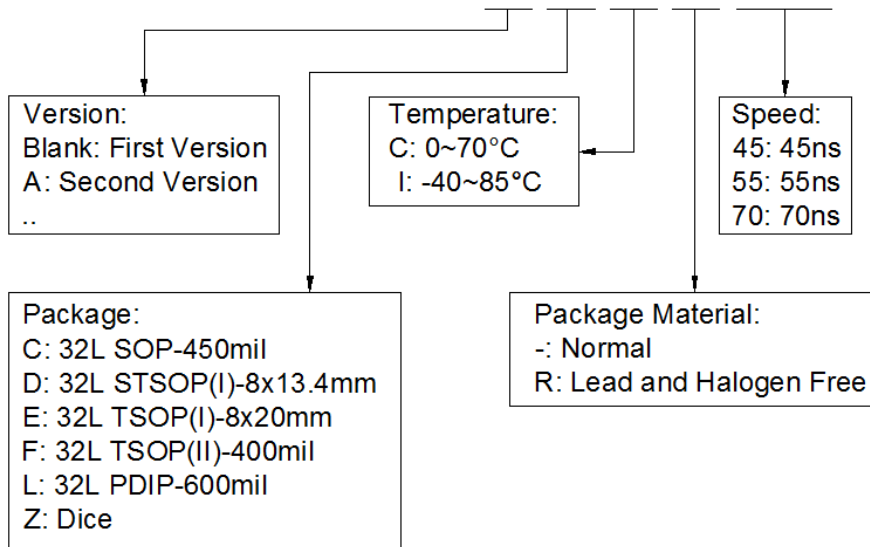
CS18LV11253

NOTES:

1. *TAS* is measured from the address valid to the beginning of write.
2. The internal write time of the memory is defined by the overlap of /CE1 and CE2 active and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. *TWR* is measured from the earlier of /CE1 or /WE going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE1 low transition or CE2 high transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.
6. /OE is continuously low (/OE = V_{IL}).
7. DOUT is the same phase of write data of this write cycle.
8. DOUT is the read data of next address.
9. If /CE1 is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500mV$ from steady state with $C_L = 5pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of /CE1 going low or CE2 going high to the end of write.

ORDER INFORMATION

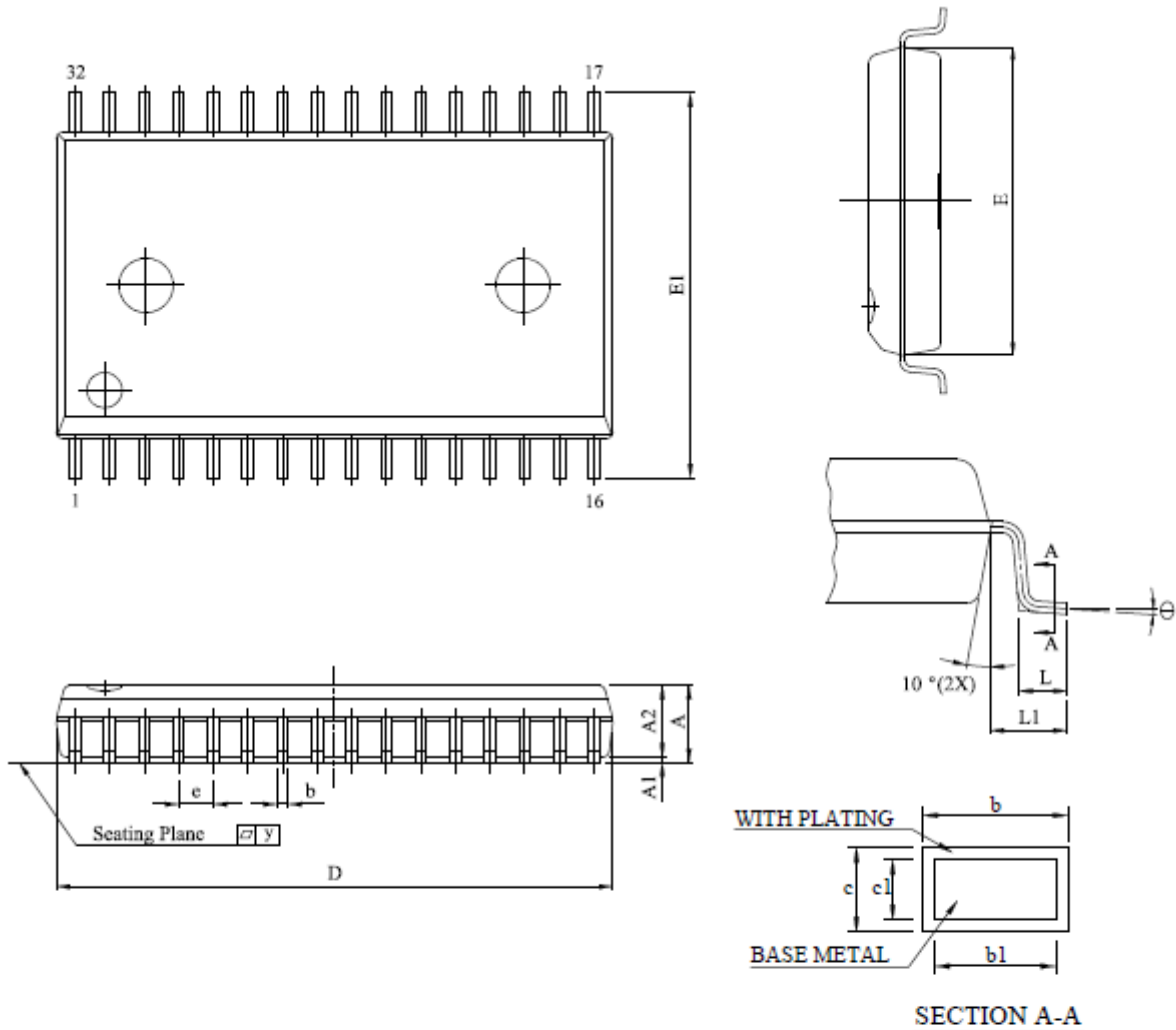
CS18LV11253 X X X X XX



Note: Package material code "R" meets ROHS

PACKAGE OUTLINE

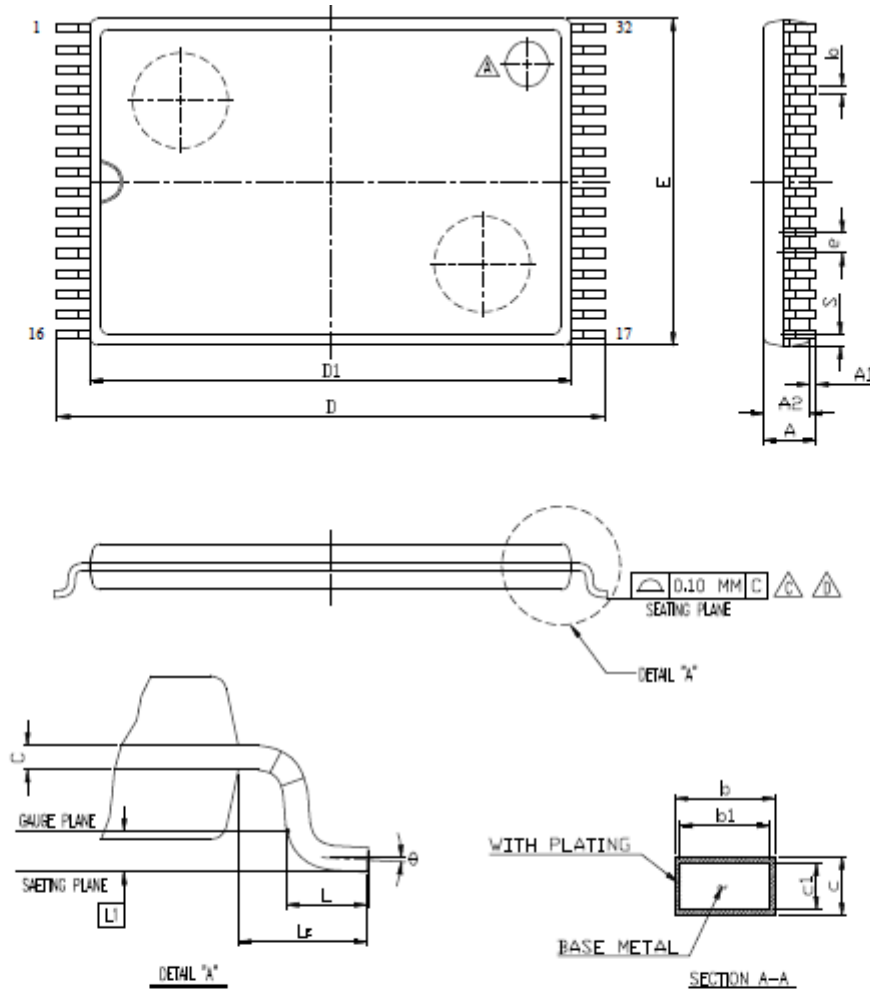
32L SOP-450mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
UNIT																
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	-	0°
	Nom.	2.821	0.229	2.680	-	-	-	-	20.447	11.303	14.097	1.270	0.834	1.397	-	-
	Max.	2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	-	0°
	Nom.	0.111	0.009	0.1055	-	-	-	-	0.805	0.445	0.555	0.050	0.033	0.055	-	-
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

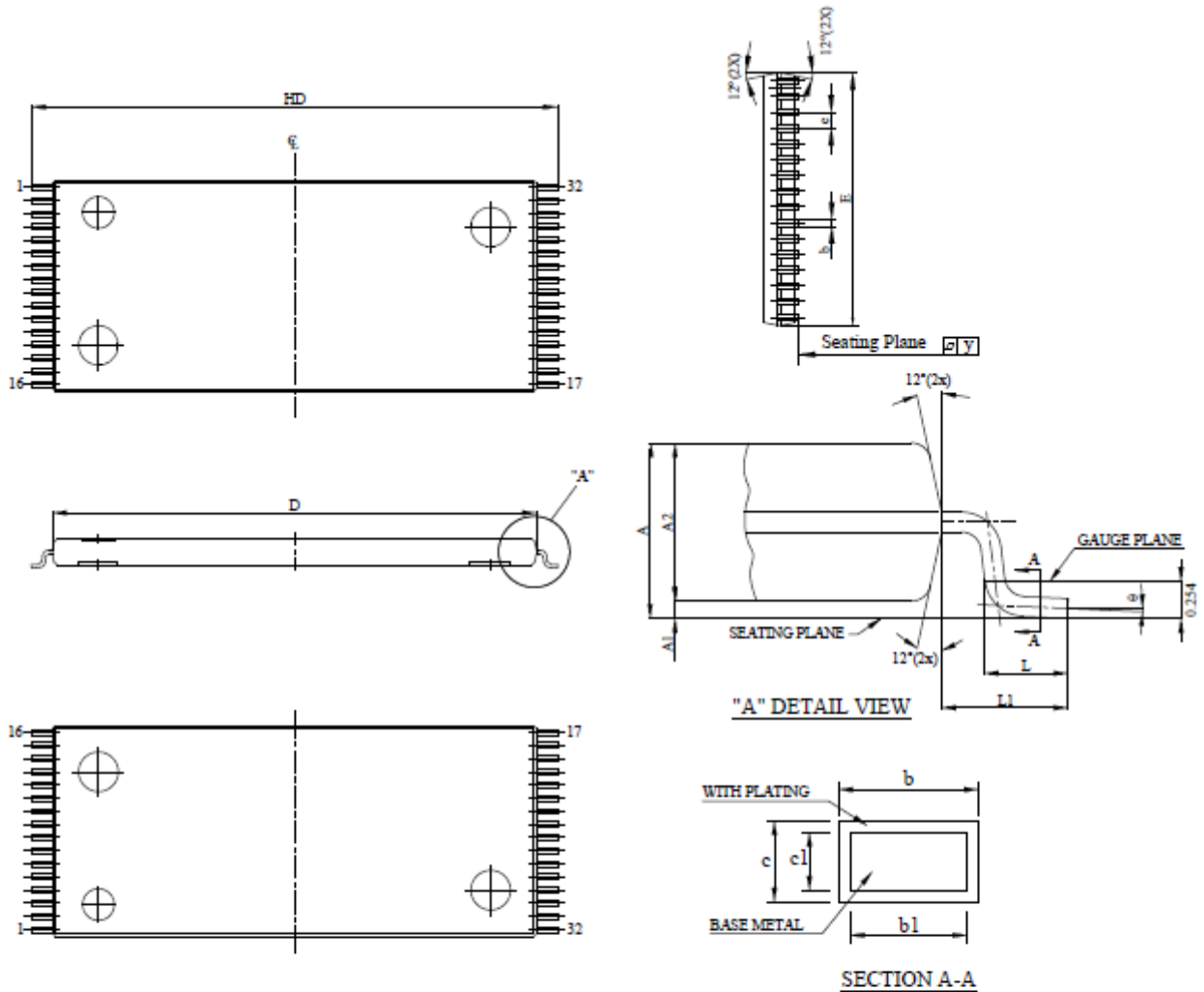
32L STSOP(I)-8x13.4mm



Note: Dimensions D1 and E do not include mold protrusions.
 D1 and E are maximum plastic body size dimensions including mold mismatch.

SYMBOL		A	A1	A2	b	b1	c	c1	E	e	D	D1	L	L1	LE	s	e
UNIT																	
mm	Min.		0.05	0.90	0.17	0.17	0.10	0.10	7.90	0.50 TYP.	13.20	11.70	0.30	0.25 BSC	0.675	0.278 TYP.	0
	Nom.			1.00	0.22	0.20	-	-	8.00		13.40	11.80	0.50				3
	Max.	1.20		1.05	0.27	0.23	0.21	0.16	8.10		13.60	11.90	0.70				5
inch	Min.		0.002	0.035	0.007	0.007	0.004	0.004	0.311	0.020 TYP.	0.520	0.461	0.012	0.010 BSC	0.027	0.0109 TYP.	0
	Nom.			0.039	0.009	0.008	-	-	0.315		0.528	0.465	0.020				3
	Max.	0.047		0.041	0.011	0.009	0.008	0.006	0.319		0.535	0.469	0.028				5

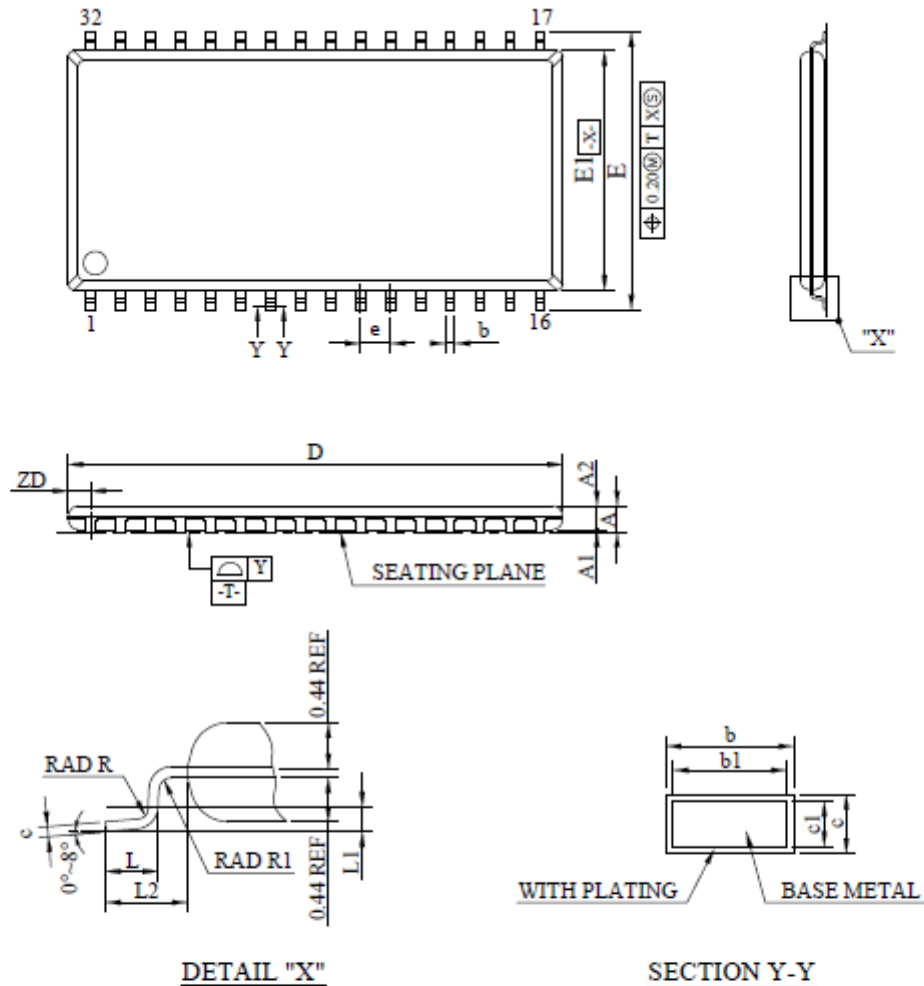
32L TSOP(I)-8x20mm



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
UNIT																
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	-	18.40	8.00	0.50	20.00	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	-	0.724	0.315	0.020	0.787	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

32L TSOP2-400mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL UNIT	A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	L2	R	R1	ZD	Y
	mm	Min. -	0.05	0.95	0.30	0.30	0.12	0.10	20.82	11.56	10.03	1.27	0.40	0.25	0.8	0.12	0.12	0.95
	Nom. -	0.10	1.00	-	0.40	-	0.127	20.95	11.76	10.16	bsc	0.50	bsc	ref	-	-	ref	-
	Max. 1.20	0.15	1.05	0.52	0.45	0.21	0.16	21.08	11.96	10.29	bsc	0.60			0.25	-		0.10
inch	Min. -	0.002	0.037	0.012	0.012	0.005	0.004	0.820	0.455	0.394	0.050	0.016	0.010	0.031	0.005	0.005	0.037	-
	Nom. -	0.004	0.039	-	0.016	-	0.005	0.825	0.463	0.400	bsc	0.020	bsc	ref	-	-	ref	-
	Max. 0.047	0.006	0.042	0.020	0.018	0.008	0.006	0.830	0.471	0.405	bsc	0.024			0.010	-		0.004