# Cover Sheet and Revision Status

| 版別 (Rev.) | DCC No. | 生效日 (Eff. Date) | 變更說明 (Change Description) | 發行人 (Originator) |
|---|---|---|---|---|
| 1.0 | 20160074 | Aug. 17, 2016 | New issue | Hank Lin |
| 2.0 | 20170013 | Jun. 22, 2017 | Revise 32L STSOP(I)-8x13.4mm package outline | Hank Lin |
| 3.0 | 20200019 | Dec. 29, 2020 | Revise ICC (operating current)<br>45ns- 20mA, 55ns- 20mA, 70ns- 15mA | Hank Lin |



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## GENERAL DESCRIPTION

The CS18LV21495 is a high performance, high speed, and super low power CMOS Static Random Access Memory organized as 262,144 words by 8 bits and operates from a wide range of 4.5 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 2uA and maximum access time of 45/55/70ns in 5.0V operation. Easy memory expansion is provided by an active LOW chip enable inputs (/CE1, CE2) and active LOW output enable (/OE) and three-state output drivers.

The CS18LV21495 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV21495 is available in JEDEC standard 32-pin sTSOP 1 -8x13.4 mm, TSOP 1 -8x20 mm, TSOP 2 –400 mil; SOP -450 mil.

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## FEATURES

- Low operation voltage : 4.5 ~ 5.5V
- Ultra low power consumption :
  - operating current: 20mA (Max.) @$t_{AA}$=45ns
  - standby current : 2uA (Typ.)
- Fast access time: 45/55/70ns (Max.)
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible, fully static operation
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE1, CE2 and /OE options.

## Product Family

| Product Family | Operating Temp | Standby (Max.) ($V_{CC}$ = 5.5V) | $V_{CC}$ Range (V) | Speed (ns) | Package Type |
|---|---|---|---|---|---|
| CS18LV21495 | 0~70°C | 10 uA | 4.5~5.5 | 45/55/70 | 32L SOP<br>32L STSOP 1<br>32L TSOP 1<br>32L TSOP 2<br>Dice |
| | -40~85°C | | | | |



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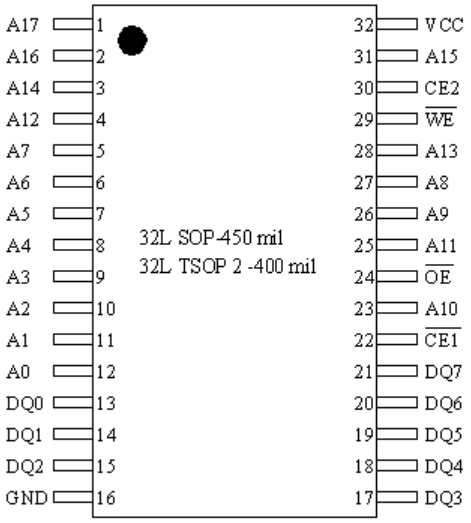
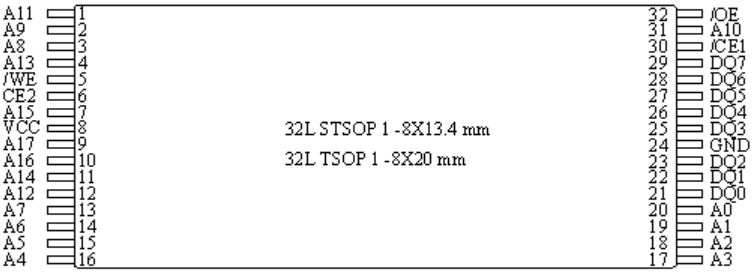
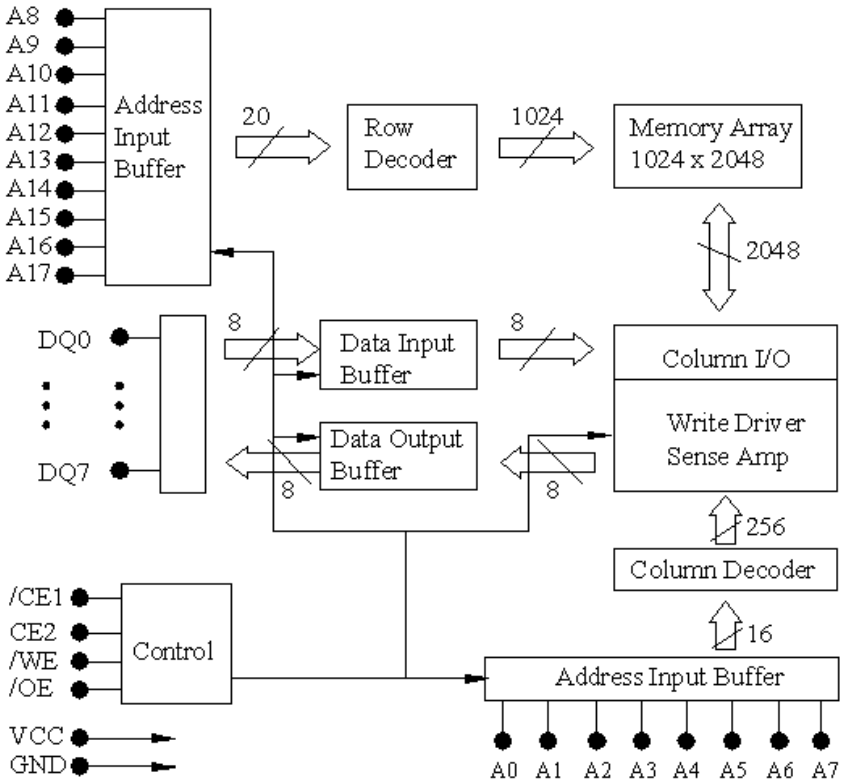
## PIN CONFIGURATIONS




## FUNCTIONAL BLOCK DIAGRAM



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## PIN DESCRIPTIONS

| Name | Type | Function |
|---|---|---|
| A0 – A17 | Input | Address inputs for selecting one of the 262,144 x 8 bit words in the RAM |
| /CE1, CE2 | Input | /CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected. |
| /WE | Input | The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location. |
| /OE | Input | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive. |
| DQ0~DQ7 | I/O | These 8 bi-directional ports are used to read data from or write data into the RAM. |
| $V_{CC}$ | Power | Power Supply |
| Gnd | Power | Ground |
| NC | | No connection |

## TRUTH TABLE

| MODE | /CE1 | CE2 | /WE | /OE | DQ0~7 | $V_{CC}$ Current |
|---|---|---|---|---|---|---|
| Standby | H | X | X | X | High Z | $I_{CCSB}$, $I_{CCSB1}$ |
| | X | L | X | X | | |
| Output Disabled | L | H | H | H | High Z | $I_{CC}$ |
| Read | L | H | H | L | $D_{OUT}$ | $I_{CC}$ |
| Write | L | H | L | X | $D_{IN}$ | $I_{CC}$ |



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## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to Vcc+0.5 | V |
| $T_{BIAS}$ | Temperature Under Bias | -40 to +125 | $^{O}C$ |
| $T_{STG}$ | Storage Temperature | -60 to +150 | $^{O}C$ |
| $P_D$ | Power Dissipation | 1.0 | W |

*1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

## OPERATING RANGE

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0~70°C | 4.5V ~ 5.5V |
| Industrial | -40~85°C | 4.5V ~ 5.5V |

## CAPACITANCE (1) (TA = 25°C, f =1.0 MHz)

| Symbol | Parameter | Conditions | MAX. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$=0V | 6 | pF |
| $C_{DQ}$ | Input/output Capacitance | $V_{I/O}$=0V | 8 | pF |

*This parameter is guaranteed and not tested.*



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## DC ELECTRICAL CHARACTERISTICS ($T_A$ = 0 to + 70°C, $V_{CC}$= 5.0V)

| Parameter Name | Parameter | Test Conduction | | MIN | TYP (1) | MAX | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Guaranteed Input Low Voltage (2) | | | -0.3 | | 0.8 | V |
| $V_{IH}$ | Guaranteed Input High Voltage (2) | | | 2.2 | | Vcc+0.5 | V |
| $I_{IL}$ | Input Leakage Current | $V_{CC}$=MAX, $V_{IN}$=0 to $V_{CC}$ | | -1 | | 1 | uA |
| $I_{OL}$ | Output Leakage Current | $V_{CC}$=MAX, /CE=$V_{IN}$, or /OE=$V_{IN}$, $V_{IO}$=0V to $V_{CC}$ | | -1 | | 1 | uA |
| $V_{OL}$ | Output Low Voltage(3) | $V_{CC}$=MAX, $I_{OL}$ = 2mA | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage(2) | $V_{CC}$=MIN, $I_{OH}$ = -1mA | | 2.4 | | | V |
| $I_{CC}$ | Operating Power Supply Current | /CE=$V_{IL}$, $I_{DQ}$=0mA, F=$F_{MAX}$ (3) | 45ns | | | 20 | mA |
| | | | 55ns | | | 20 | |
| | | | 70ns | | | 15 | |
| $I_{CCSB}$ | Standby Supply - TTL | /CE=$V_{IH}$, $I_{DQ}$=0mA, | | | | 0.3 | mA |
| $I_{CCSB1}$ | Standby Current -CMOS | /CE≧$V_{CC}$-0.2V, $V_{IN}$≧$V_{CC}$-0.2V or $V_{IN}$≦0.2V | | | 2 | 10 | uA |

1. *Typical characteristics are at TA = 25°C.*
2. *Overshoot: $V_{CC}$ +2.0V in case of pulse width ≦20ns.*
3. *Undershoot: - 2.0V in case of pulse width ≦20ns.*
4. *Overshoot and undershoot are sampled, not 100% tested.*



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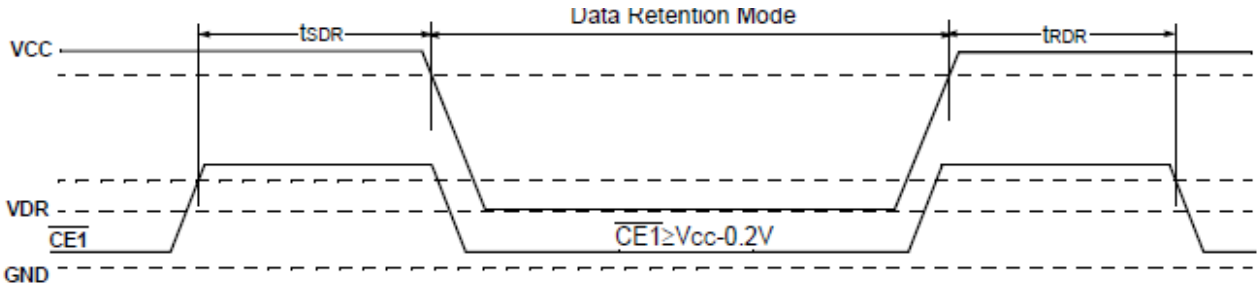
## DATA RETENTION CHARACTERISTICS ($T_A$ = 0 to + 70°C)

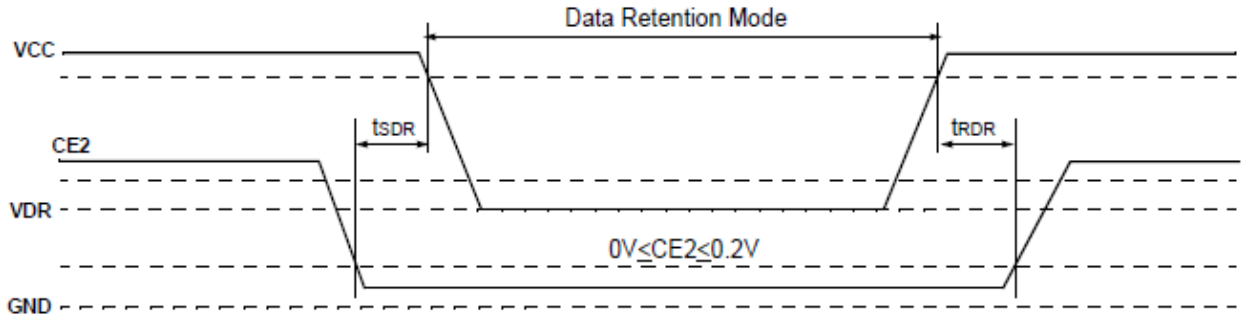
| Parameter Name | Parameter | Test Conduction | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | /CE≧$V_{CC}$-0.2V, $V_{IN}$≧$V_{CC}$-0.2V or $V_{IN}$≦0.2V | 1.5 | | | V |
| $I_{CCDR}$ | Data Retention Current | /CE≧$V_{CC}$-0.2V, $V_{CC}$=1.5V $V_{IN}$≧$V_{CC}$-0.2V or $V_{IN}$≦0.2V | | 2 | 6 | uA |
| $T_{CDR}$ | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | | | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$ (1) | | | ns |

*1. Read Cycle Time.*

### LOW $V_{CC}$ DATA RETENTION WAVEFORM (1) (/CE1 Controlled)




### LOW $V_{CC}$ DATA RETENTION WAVEFORM (2) (CE2 Controlled)



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## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | Vcc/0V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Level | 0.5Vcc |
| Output Load | See FIGURE 1A and 1B |

## KEY TO SWITCHING WAVEFORMS

| WAVEFORMS | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | MUST BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGE FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGE FROM L TO H |
| | DON'T CARE ANY CHANGE PERMITTED | CHANGE STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE OFF STATE |

## AC TEST LOADS AND WAVEFORMS

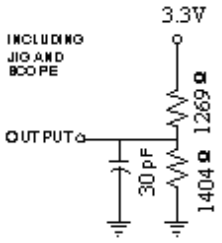


FIGURE 1A

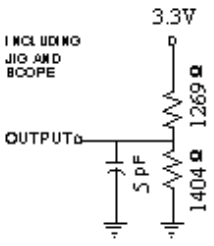


FIGURE 1B

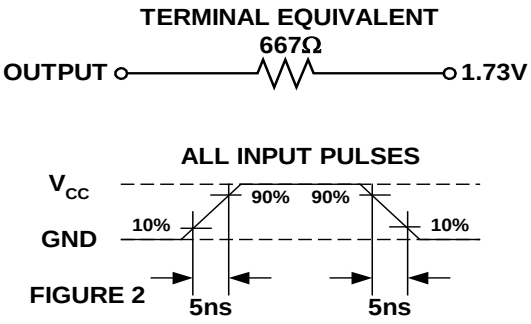


FIGURE 2



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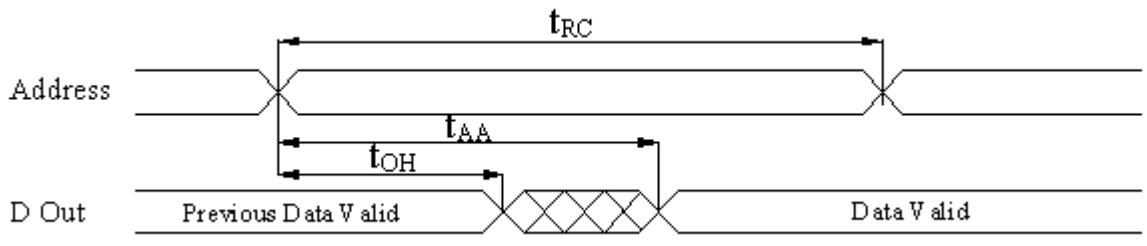
## AC ELECTRICAL CHARACTERISTICS ($T_A$ = 0 to + 70°C, $V_{CC}$ = 5.0V)

### < READ CYCLE >

| JEDEC Parameter Name | Parameter Name | Description | 45ns | | 55ns | | 70ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{AVAX}$ | $t_{RC}$ | Read Cycle Time | 45 | | 55 | | 70 | | ns |
| $t_{AVQV}$ | $t_{AA}$ | Address Access Time | | 45 | | 55 | | 70 | ns |
| $t_{ELQV}$ | $t_{CO}$ | Chip Select Access Time | | 45 | | 55 | | 70 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Valid | | 22 | | 25 | | 35 | ns |
| $t_{ELQX}$ | $t_{LZ}$ | Chip Select to Output Low Z | 10 | | 10 | | 10 | | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable to Output in Low Z | 5 | | 5 | | 5 | | ns |
| $t_{EHQZ}$ | $t_{CHZ}$ | Chip Deselect to Output in High Z | | 18 | | 20 | | 25 | ns |
| $t_{GHQZ}$ | $t_{OHZ}$ | Output Disable to Output in High Z | | 18 | | 20 | | 25 | ns |
| $t_{AXOX}$ | $t_{OH}$ | Out Disable to Address Change | 10 | | 10 | | 10 | | ns |

## SWITCHING WAVEFORMS (READ CYCLE)

### READ CYCLE 1



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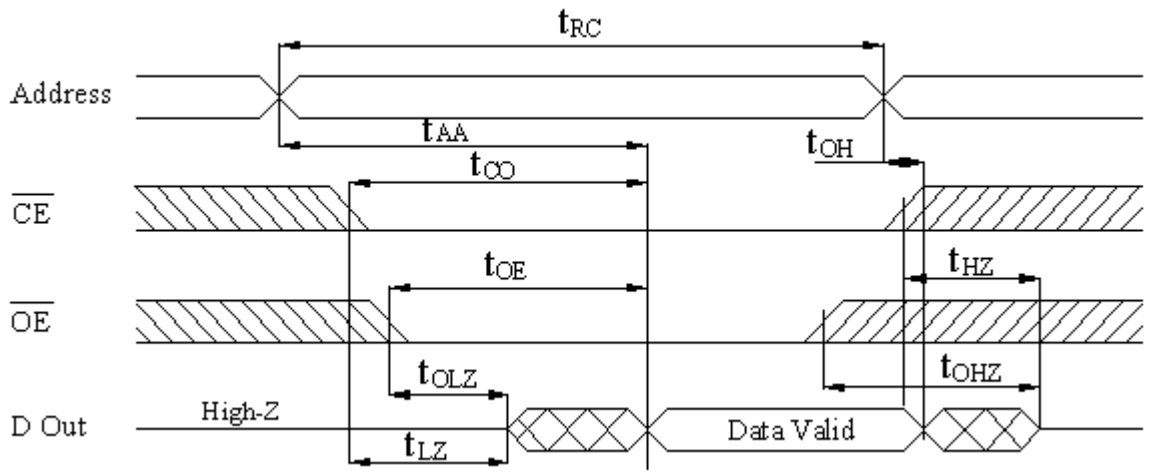
### READ CYCLE 2




*NOTES:*

1. *$t_{HZ}$ and $t_{OHZ}$ are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *At any given temperature and voltage condition, $t_{HZ}$ (Max.) is less than $t_{LZ}$ (Min.) both for a given device and from device to device interconnection.*

## AC ELECTRICAL CHARACTERISTICS ($T_A$ = 0 to + 70°C, $V_{CC}$ = 5.0V)

### < WRITE CYCLE >

| JEDEC Parameter Name | Parameter Name | Description | 45ns | | 55ns | | 70ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{AVAX}$ | $t_{WC}$ | Write Cycle Time | 45 | | 55 | | 70 | | ns |
| $t_{E1LWH}$ | $t_{CW}$ | Chip Select to End of Write | 35 | | 45 | | 60 | | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{AVWH}$ | $t_{AW}$ | Address Valid to End of Write | 35 | | 45 | | 60 | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | 35 | | 40 | | 55 | | ns |
| $t_{WHAX}$ | $t_{WR}$ | Write Recovery Time | 0 | | 0 | | 0 | | ns |
| $t_{WLQZ}$ | $t_{WHZ}$ | Write to Output in High Z | | 18 | | 20 | | 25 | ns |
| $t_{DVWH}$ | $t_{DW}$ | Data to Write Time Overlap | 25 | | 25 | | 30 | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold from Write Time | 0 | | 0 | | 0 | | ns |
| $t_{WHOX}$ | $t_{OW}$ | End of Write to Output Active | 5 | | 5 | | 5 | | ns |



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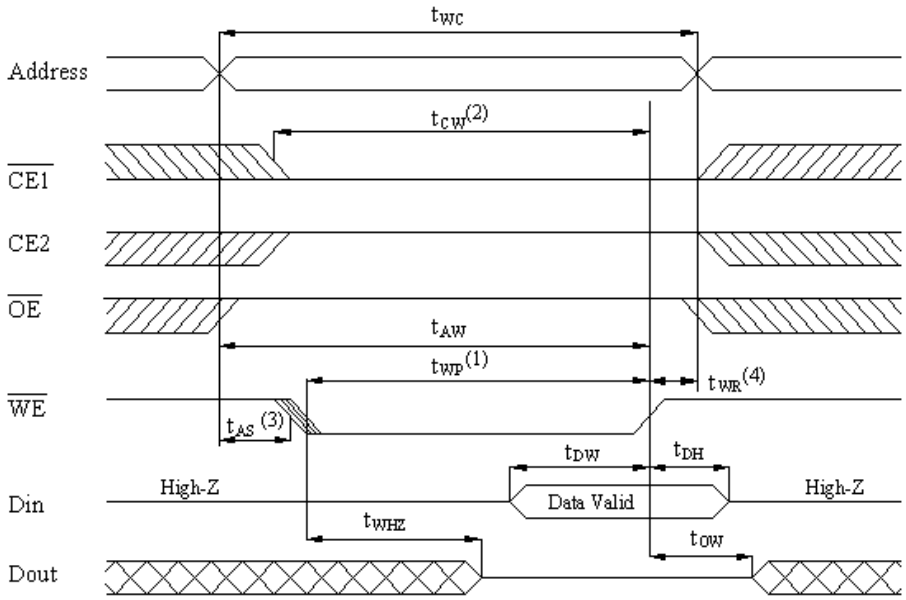
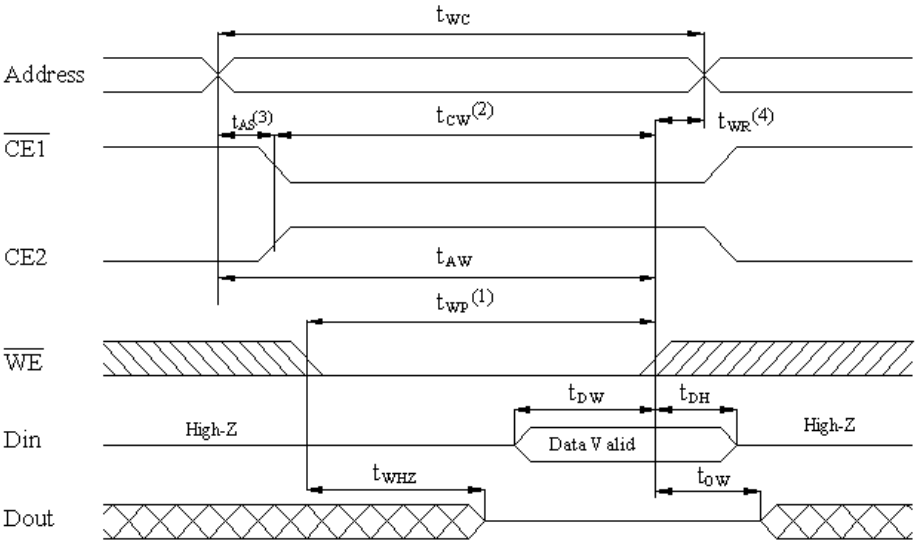
## SWITCHING WAVEFORMS (WRITE CYCLE)

### WRITE CYCLE 1 (/WE controlled)




### WRITE CYCLE 2 (/CE1 and CE2 controlled)




*NOTES:*

1. *A write occurs during the overlap ($t_{WP}$) of low /CE1, a high CE2 and low /WE. A write begins when /CE1 goes low, CE2 going high and /WE goes low. A write ends at the earliest transition when /CE1 goes high, CE2 goes high an /WE goes high. The tWP is measured from the*



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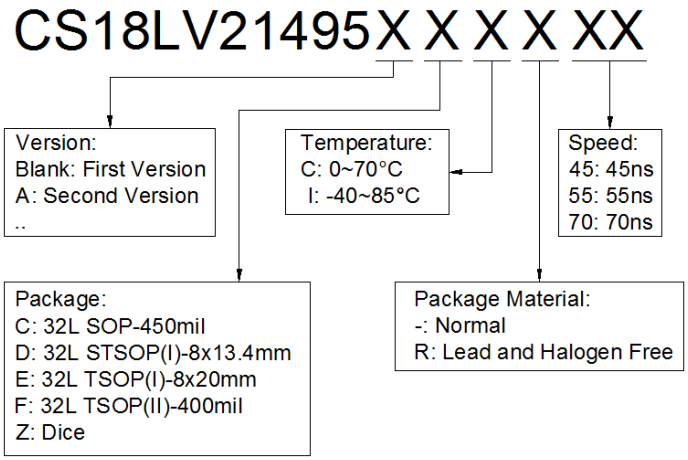
*beginning of the write to the end of write.*

2. *$t_{CW}$ is measured from the /CE1 going low or CE2 going low to end of write.*
3. *$t_{AS}$ is measured from the address valid to the beginning of write.*
4. *$t_{WR}$ is measured from the end or write to the address change. TWR applied in case a write ends as /CE1 or /WE going high or CE2 going low.*

## ORDER INFORMATION




*Note: Package material code "R" meets ROHS*



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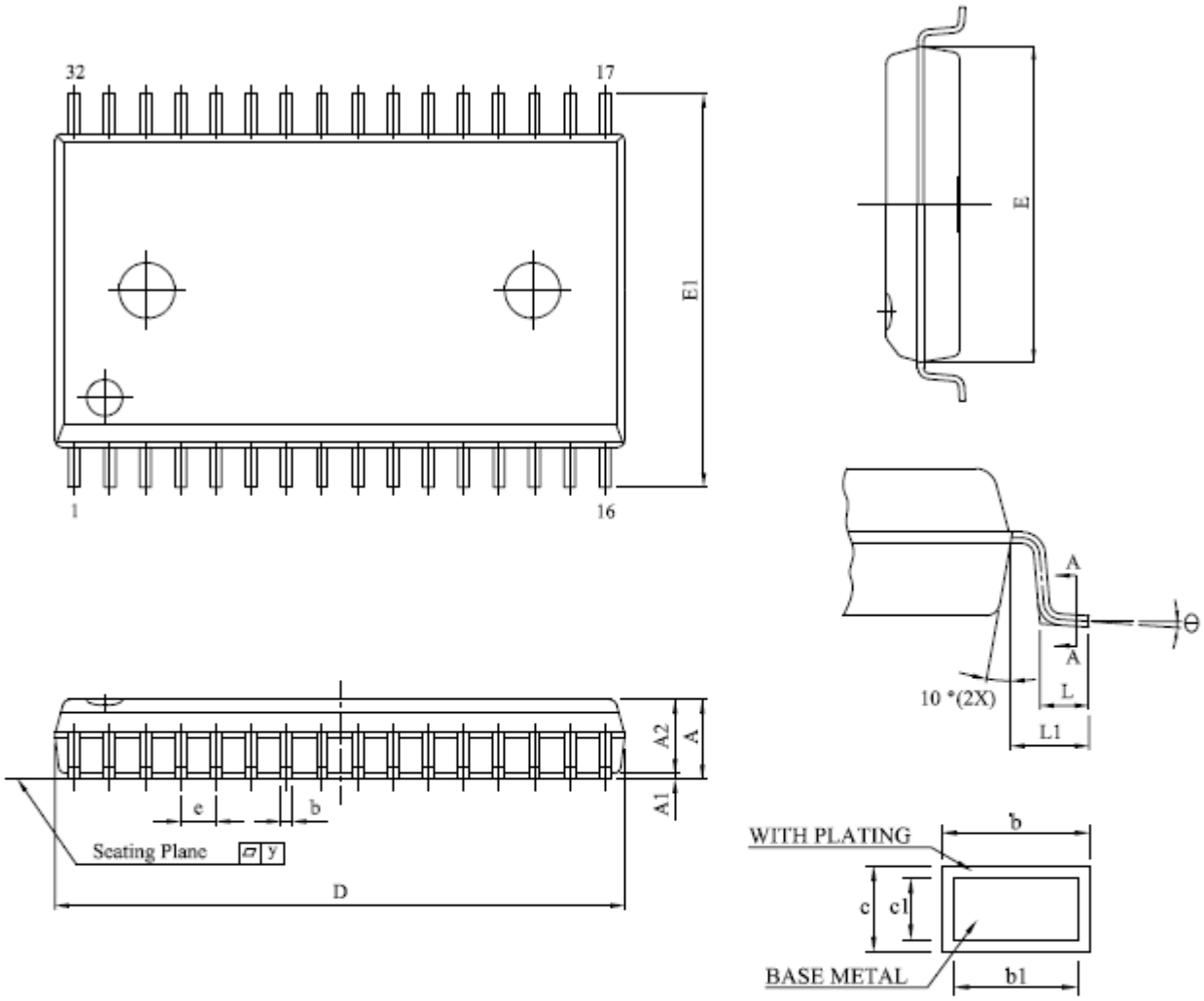
## PACKAGE OUTLINE

### 32L SOP-450mil




Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

| SYMBOL / UNIT | | A | A1 | A2 | b | b1 | c | c1 | D | E | E1 | e | L | L1 | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 2.645 | 0.102 | 2.540 | 0.35 | 0.35 | 0.15 | 0.15 | 20.320 | 11.176 | 13.792 | 1.118 | 0.584 | 1.194 | – | 0° |
| | Nom. | 2.821 | 0.229 | 2.680 | – | – | – | – | 20.447 | 11.303 | 14.097 | 1.270 | 0.834 | 1.397 | – | – |
| | Max. | 2.997 | 0.356 | 2.820 | 0.50 | 0.46 | 0.32 | 0.28 | 20.574 | 11.430 | 14.402 | 1.422 | 1.084 | 1.600 | 0.1 | 10° |
| inch | Min. | 0.104 | 0.004 | 0.1000 | 0.014 | 0.014 | 0.006 | 0.006 | 0.800 | 0.440 | 0.543 | 0.044 | 0.023 | 0.047 | – | 0° |
| | Nom. | 0.111 | 0.009 | 0.1055 | – | – | – | – | 0.805 | 0.445 | 0.555 | 0.050 | 0.033 | 0.055 | – | – |
| | Max. | 0.118 | 0.014 | 0.1110 | 0.020 | 0.018 | 0.012 | 0.011 | 0.810 | 0.450 | 0.567 | 0.056 | 0.043 | 0.063 | 0.004 | 10° |



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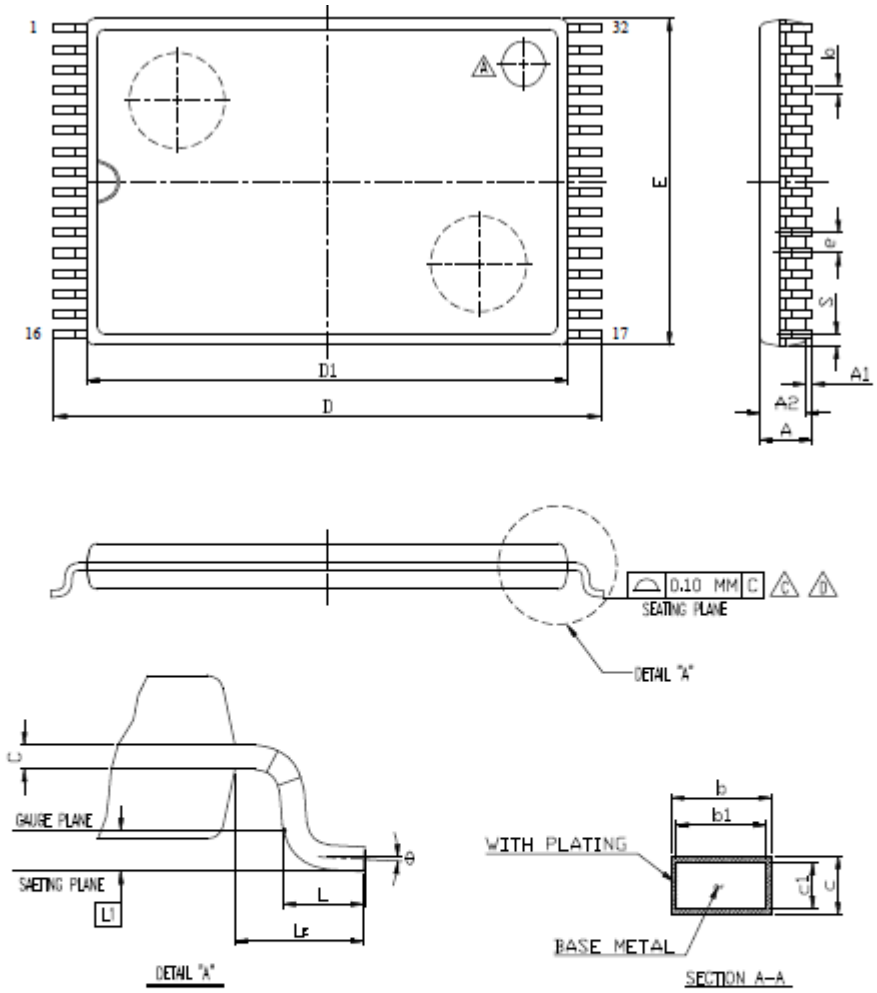
## 32L STSOP(I)-8x13.4mm




Note: Dimensions D1 and E do not include mold protrusions.
D1 and E are maximun plastic body size dimensions including mold mismatch.

| SYMBOL / UNIT | | A | A1 | A2 | b | b1 | c | c1 | E | e | D | D1 | L | L1 | LE | S | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | | 0.05 | 0.90 | 0.17 | 0.17 | 0.10 | 0.10 | 7.90 | 0.50 TYP. | 13.20 | 11.70 | 0.30 | 0.25 BSC | 0.675 | 0.278 TYP. | 0 |
| | Nom. | | | 1.00 | 0.22 | 0.20 | – | – | 8.00 | | 13.40 | 11.80 | 0.50 | | | | 3 |
| | Max. | 1.20 | | 1.05 | 0.27 | 0.23 | 0.21 | 0.16 | 8.10 | | 13.60 | 11.90 | 0.70 | | | | 5 |
| inch | Min. | | 0.002 | 0.035 | 0.007 | 0.007 | 0.004 | 0.004 | 0.311 | 0.020 TYP. | 0.520 | 0.461 | 0.012 | 0.010 BSC | 0.027 | 0.0109 TYP. | 0 |
| | Nom. | | | 0.039 | 0.009 | 0.008 | – | – | 0.315 | | 0.528 | 0.465 | 0.020 | | | | 3 |
| | Max. | 0.047 | | 0.041 | 0.011 | 0.009 | 0.008 | 0.006 | 0.319 | | 0.535 | 0.469 | 0.028 | | | | 5 |



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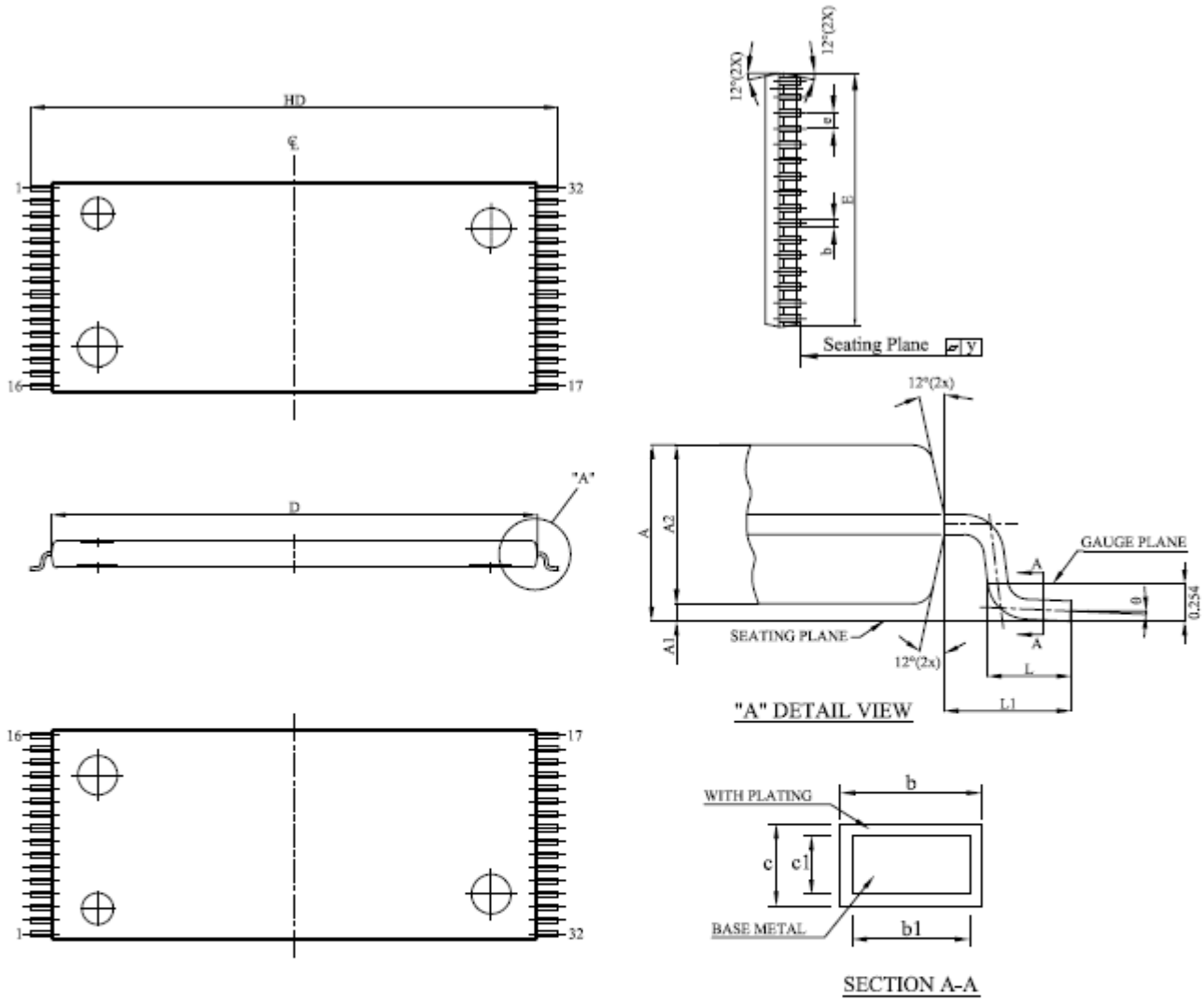
**32L TSOP(I)-8x20mm**




Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

| SYMBOL / UNIT | | A | A1 | A2 | b | b1 | c | c1 | D | E | e | HD | L | L1 | y | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 1.00 | 0.05 | 0.95 | 0.17 | 0.17 | 0.10 | 0.10 | 18.30 | 7.90 | 0.40 | 19.80 | 0.40 | 0.70 | – | 0° |
| | Nom. | 1.10 | 0.10 | 1.00 | 0.22 | 0.20 | – | – | 18.40 | 8.00 | 0.50 | 20.00 | 0.50 | 0.80 | – | – |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.23 | 0.21 | 0.16 | 18.50 | 8.10 | 0.60 | 20.20 | 0.70 | 0.90 | 0.1 | 8° |
| inch | Min. | 0.0393 | 0.002 | 0.037 | 0.007 | 0.007 | 0.004 | 0.004 | 0.720 | 0.311 | 0.016 | 0.779 | 0.0157 | 0.0275 | – | 0° |
| | Nom. | 0.0433 | 0.004 | 0.039 | 0.009 | 0.008 | – | – | 0.724 | 0.315 | 0.020 | 0.787 | 0.0197 | 0.0315 | – | – |
| | Max. | 0.0473 | 0.006 | 0.041 | 0.011 | 0.009 | 0.008 | 0.006 | 0.728 | 0.319 | 0.024 | 0.795 | 0.0277 | 0.0355 | 0.004 | 8° |



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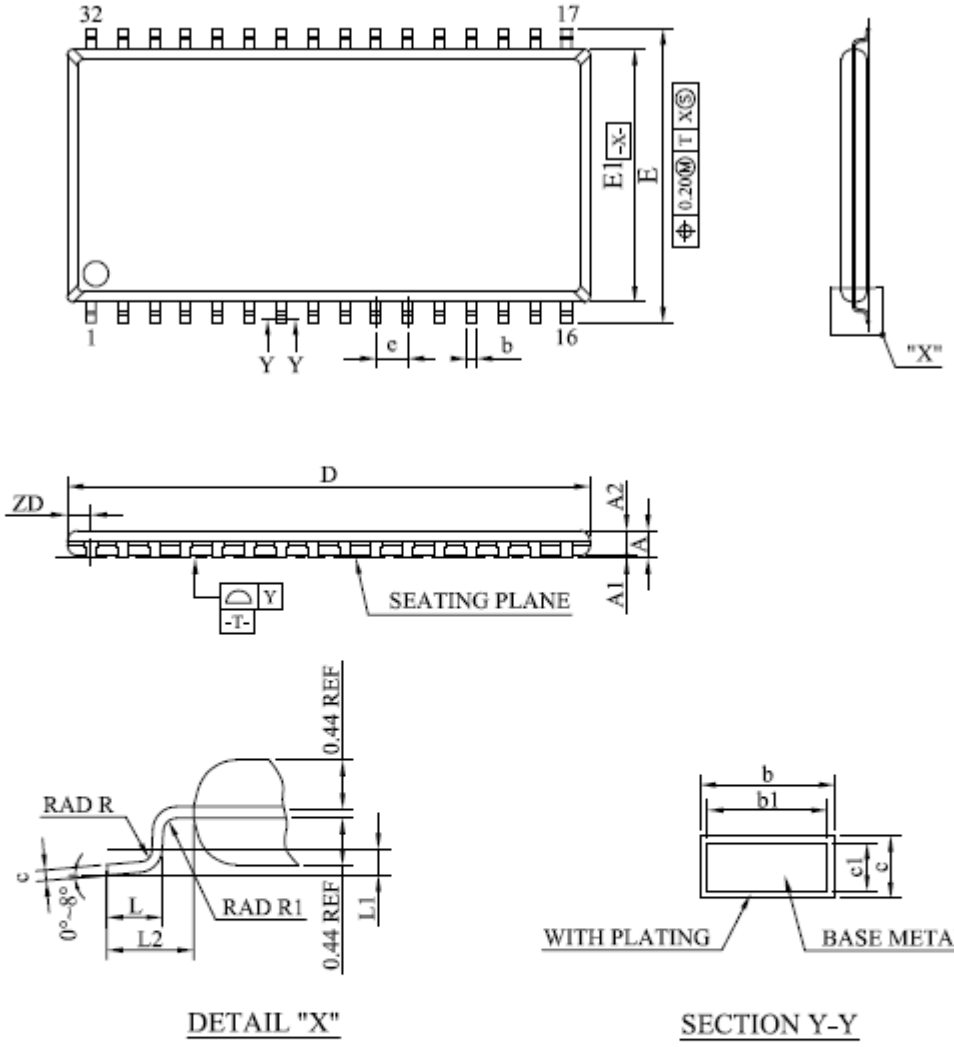
## 32L TSOP2-400mil




DETAIL "X"

SECTION Y-Y

Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

| SYMBOL / UNIT | | A | A1 | A2 | b | b1 | c | c1 | D | E | E1 | e | L | L1 | L2 | R | R1 | ZD | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | – | 0.05 | 0.95 | 0.30 | 0.30 | 0.12 | 0.10 | 20.82 | 11.56 | 10.03 | 1.27 bsc | 0.40 | 0.25 bsc | 0.8 ref | 0.12 | 0.12 | 0.95 ref | – |
| | Nom. | – | 0.10 | 1.00 | – | 0.40 | – | 0.127 | 20.95 | 11.76 | 10.16 | | 0.50 | | | – | – | | – |
| | Max. | 1.20 | 0.15 | 1.05 | 0.52 | 0.45 | 0.21 | 0.16 | 21.08 | 11.96 | 10.29 | | 0.60 | | | 0.25 | – | | 0.10 |
| inch | Min. | – | 0.002 | 0.037 | 0.012 | 0.012 | 0.005 | 0.004 | 0.820 | 0.455 | 0.394 | 0.050 bsc | 0.016 | 0.010 bsc | 0.031 ref | 0.005 | 0.005 | 0.037 ref | – |
| | Nom. | – | 0.004 | 0.039 | – | 0.016 | – | 0.005 | 0.825 | 0.463 | 0.400 | | 0.020 | | | – | – | | – |
| | Max. | 0.047 | 0.006 | 0.042 | 0.020 | 0.018 | 0.008 | 0.006 | 0.830 | 0.471 | 0.405 | | 0.024 | | | 0.010 | – | | 0.004 |



Chiplus reserves the right to change product or specification without notice.