Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20180019	5/29-2018	New issue	Hank Lin
2.0	20190004	1/31-2019	Revise power on timing drawing	Hank Lin
3.0	20200018	12/7-2020	Revise Read /Write Timing Charts	Hank Lin
4.0	20210025	6/24-2021	Revise V_{CC} range from 2.7~3.6V to 2.7~3.3V	Hank Lin

■ Product Description

The CS26LV16173 is a high performance, high speed, low power pseudo SRAM organized as 1M words by 16 bits and operates from a wide range of 2.7 to 3.3V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and maximum access time of 70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers. The CS26LV16173 has the page access operation, page size is 16 words, and has a deep power down feature, reducing the power consumption significantly when chip is deselected. The CS26LV16173 is available 48-ball TFBGA package.

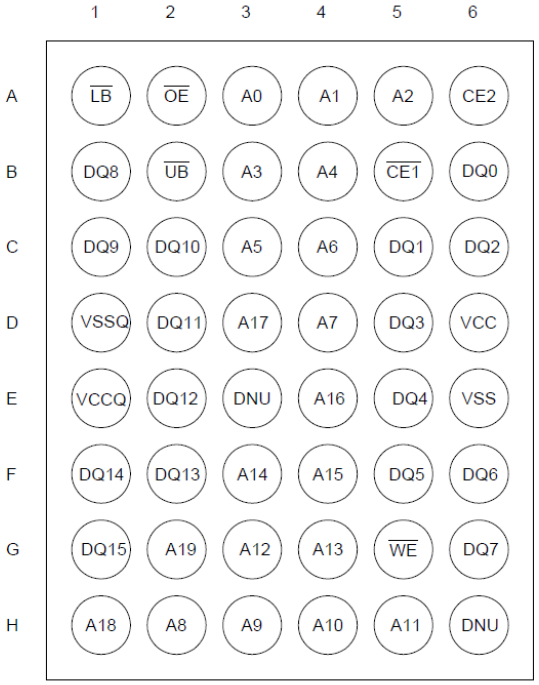
■ Features

- Single power supply voltage of 2.7 to 3.3V
- Direct TTL compatibility for all inputs and outputs.
- Deep power-down mode: Memory cell data invalid.
- Page operation mode
- Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  - Standby 120 uA(Max)
  - Deep power-down standby 15 uA (Max.)
- Access Time
  - /CE1 Access Time: 70ns
  - /OE Access Time: 25ns
  - Page Access Time: 25ns

■ Product Family

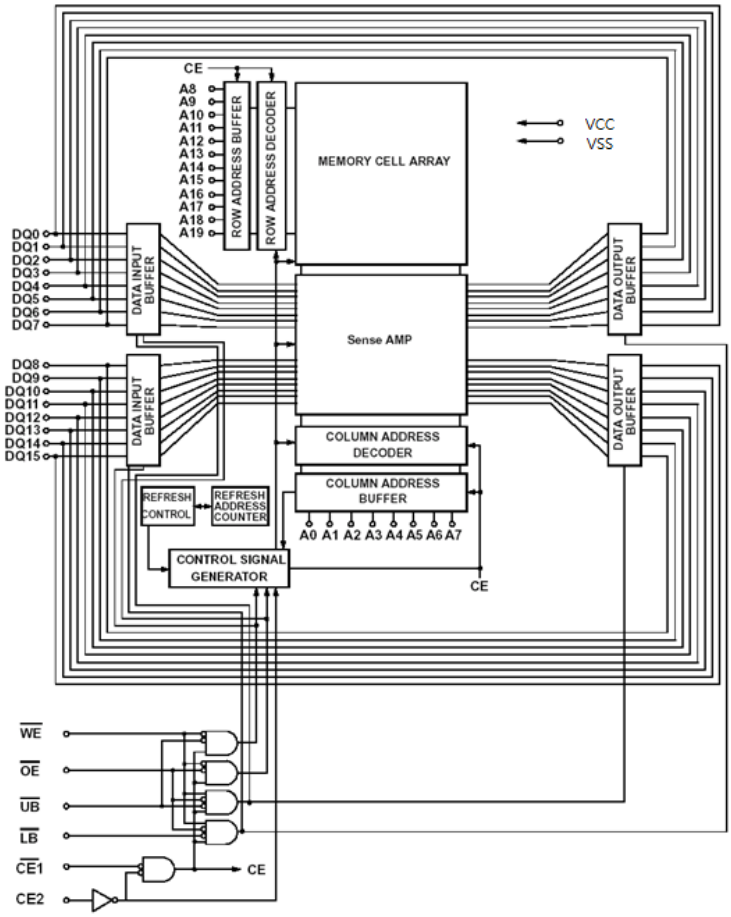
Product Family	Operating Temp	Vcc. Range	Speed(ns)	Standby (Max.)	Package Type
CS26LV16173	0~70°C	2.7~3.3	70	120 uA	48ball TFBGA-6*8mm
	-40~85°C				

Pin Configuration



48 TFBGA - Top View

■ Functional Block Diagram



■ Pin Descriptions

Name	Type	Function
A0~A19	input	Address input
CE1	input	Chip Enable Input1, Low : Enable
CE2	input	Chip Enable Input2, High: Enable, Low: Enter Power Down mode
/WE	input	Write Enable input, Low :Enable
/OE	input	Output Enable input, Low :Enable
/LB	input	Lower byte write control
/UB	input	Upper byte write control
DQ0~DQ15	I/O	Data inputs/outputs
V_{CC}	Power	Device Power supply
V_{SS}	Power	V_{SS} must be connected ground
V_{CCQ}	Power	I/O Power supply
V_{SSQ}	Power	V_{SSQ} must be connected ground
DNU		Do not use

■ Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V_{CC} Current
Standby	H	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC}
Upper Byte Read					L	H	D_{OUT}	High Z	I_{CC}
Lower Byte Read					H	L	High Z	D_{OUT}	I_{CC}
Write	L	H	H	L	L	L	D_{IN}	D_{IN}	I_{CC}
Upper Byte Write					L	H	D_{IN}	Invalid	I_{CC}
Lower Byte Write					H	L	Invalid	D_{IN}	I_{CC}

Note: X means don't care. (Must be low or high state)

■ Absolute Maximum Ratings(1)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	-0.2 to Vcc+0.3	V
V_{OUT}	Output Voltage	-0.2 to Vcc+0.3	
V_{CC}	Device Power Supply Voltage	-0.2 to 3.3	V
T_{STG}	Storage Temperature	-65 to +150	^{O}C
T_A	Operating Temperature	-40 to +85	^{O}C
P_D	Power Dissipation	1.0	W

1. Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device.

Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Revommended DC Operating Conditions

(T_A = 0 to + 70°C , V_{CC}= 3.0V)

Item	Symbol	CS26LV16173			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	2.7	3.0	3.3	V
I/O operating voltage ($V_{CCQ} \le V_{CC}$)	V_{CCQ}	2.7	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	0.7V_{CCQ}	V_{CC}	V_{CC}+0.2[1)]	V
Input low voltage	V_{IL}	-0.2[2)]	0	0.2V_{CCQ}	V

Note :

1. Overshoot : Vcc+1.0V in case of pulse width≤20ns.
2. Undershoot : -1.0V in case of pulse width≤20ns.
3. Overshoot and undershoot are sampled, not 100% tested.

■ DC and Operating Characteristics

Iten	Symbol	Test Conditions	Min.	Typ	Max.	unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1	-	1	uA
Output leakage current	I_{LO}	/CS=V_{IH}, /ZZ=V_{IH}, /OE=V_{IH} or /WE=V_{IL}, VIO=V_{SS} to VCC	-1	-	1	uA
Average operating current	$I_{CC!}$	Cycle time=1us, 100%duty, IIO=0mA, /CS≤0.2V, /ZZ=V_{IH}, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	-	-	3	mA
	I_{CC2}	Cycle time=Min, IIO=0mA, 100% duty, /CS=V_{IL}, /ZZ=V_{IH}, VIN=V_{IL} or V_{IH}	-	-	20	mA
Page mode operating current	I_{CCP}	Cycle time=Min (t_{RC}, t_{PC}), IIO=0mA, 100% duty, /CS=V_{IL}, /ZZ=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	15	mA
Output low voltage	V_{OL}	I_{OL}=0.5mA			0.2* V_{CCQ}	V
Output high voltage	V_{OH}	I_{OH}=-0.5mA	0.8* V_{CCQ}			V
Standby Current(TTL)	I_{SB}	/CS=V_{IH}, /ZZ=V_{IH}, Other inputs=V_{IH} or V_{IL}	-	-	0.3	mA
Standby Current(CMOS)	I_{SB1}	/CS≥VCC-0.2V, /ZZ≥VCC-0.2V, Other inputs=0~V_{CC}	-	-	120	uA
Deep Power Down Modes	I_{SB0}	/ZZ≤0.2V, Other inputs=0~V_{CC}, No refresh(DPD)	-	-	15	uA

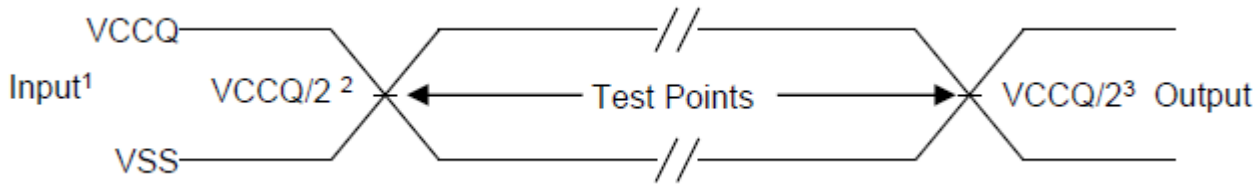
■ Capacitance (1)

(TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	Min.	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	2	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	3.5	5	pF

1. This parameter is sampled periodically and is not 100% tested

■ AC Input/Output Reference Waveform



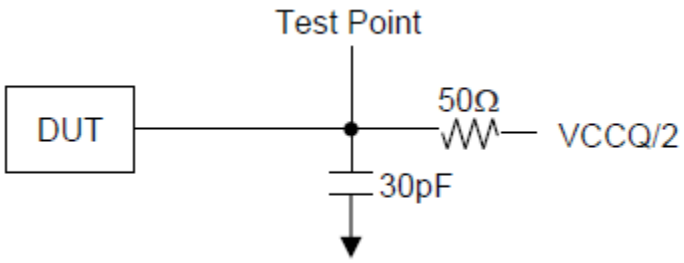
NOTE:

1. AC test inputs are driven at V_{CCQ} for a logic 1 and V_{SS} for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.

2. Input timing begins at V_{CCQ}/2.

3. Output timing ends at V_{CCQ}/2.

■ AC Test Conditions



■ AC Characteristicts

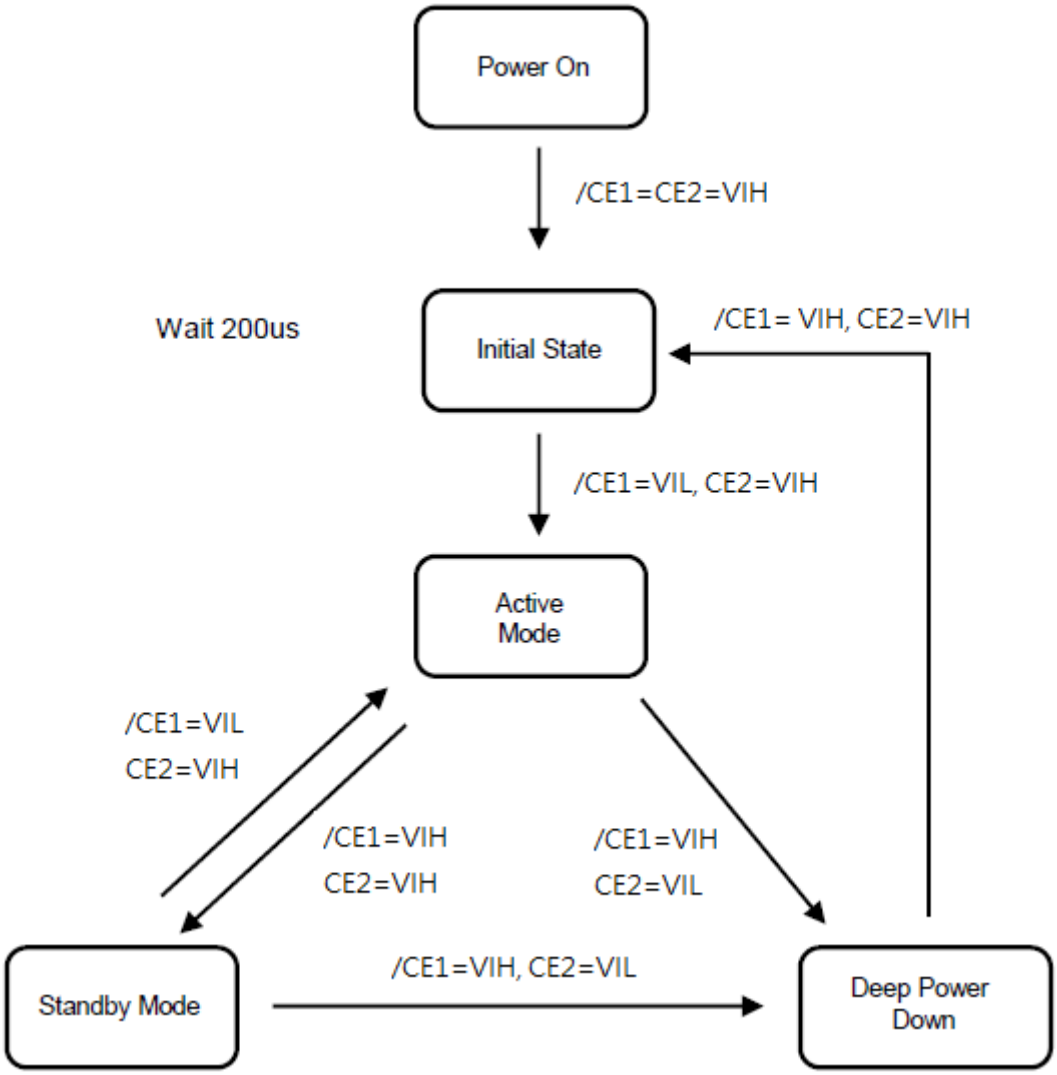
(V_{CC}=2.7V~3.6V, Commercial product: TA=-0 to 70 °C , Industrial product : TA=-40 to 85 °C)

Parameter List		Symbol	70ns		Units
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	20	ns
	/UB, /LB Access Time	t_{BA}	-	25	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	/UB, /LB Enable to Low-Z Output	t_{BLZ}	0	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	0	-	ns
	Chip Disable to High- Z Output	t_{HZ}	0	8	ns
	/UB, /LB Disable to High- Z Output	t_{BHZ}	0	8	ns
	Output Disable to High- Z Output	t_{OHZ}	0	8	ns
	Output Hold from Address Change	t_{OH}	5	-	ns
Write	Write Cycle Time	t_{WC}	70	20k	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	/UB, /LB Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	50	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	8	ns
	Data to Write Time Overlap	t_{DW}	20	-	ns
	Data Hold from Write Time	tDH	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns
Page	Page Mode Cycle Time	t_{PC}	25	-	ns
	Page Mode Address Access Time	t_{PAA}	-	25	ns
	Maximum Cycle Time	t_{MRC}	-	20k	ns
/CS High Pulse Width		t_{CP}	10	-	ns

■ Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CE1=CE2=V_{IH}

■ Standby Mode State machines

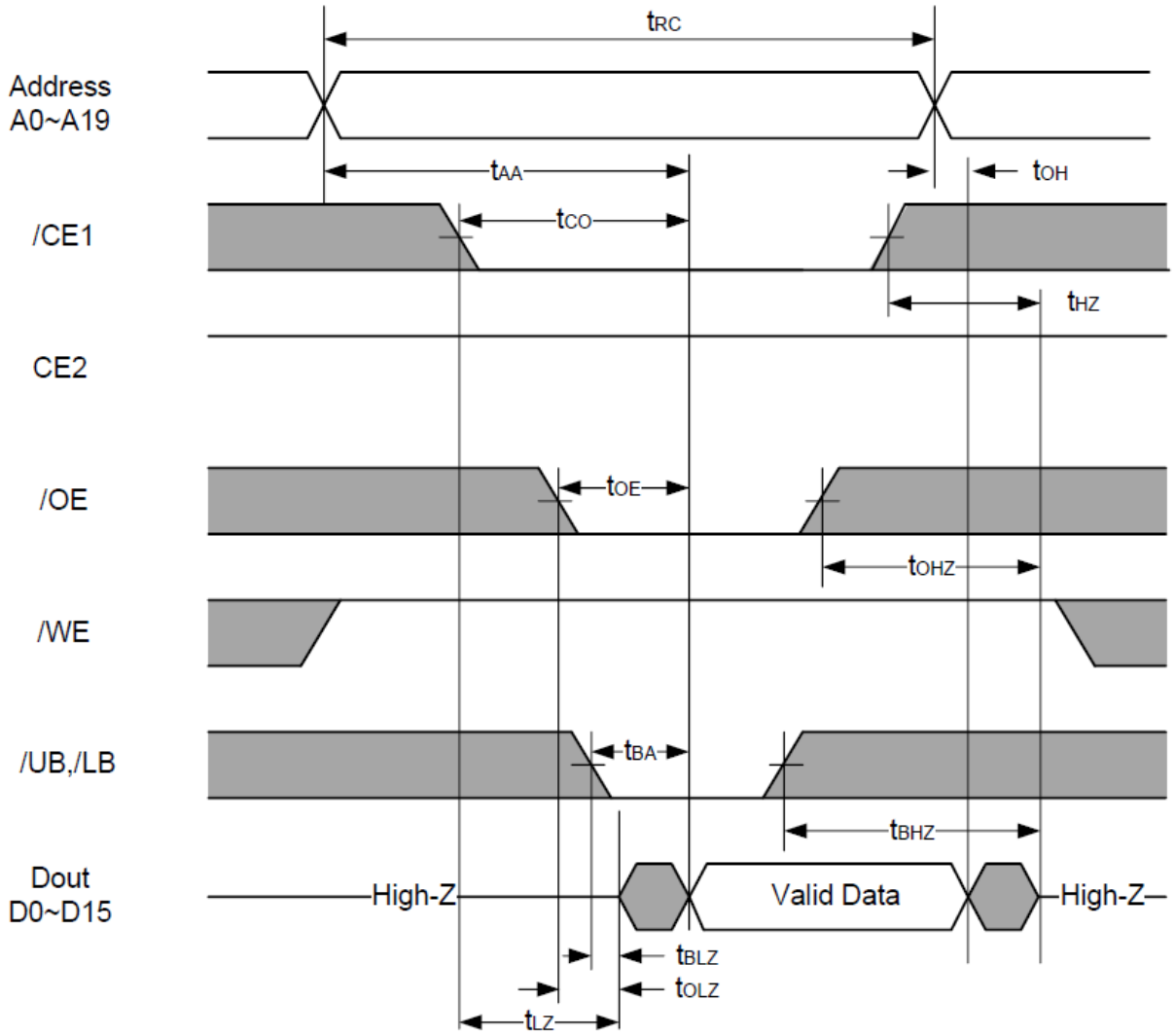


■ Standby Mode Characteristics

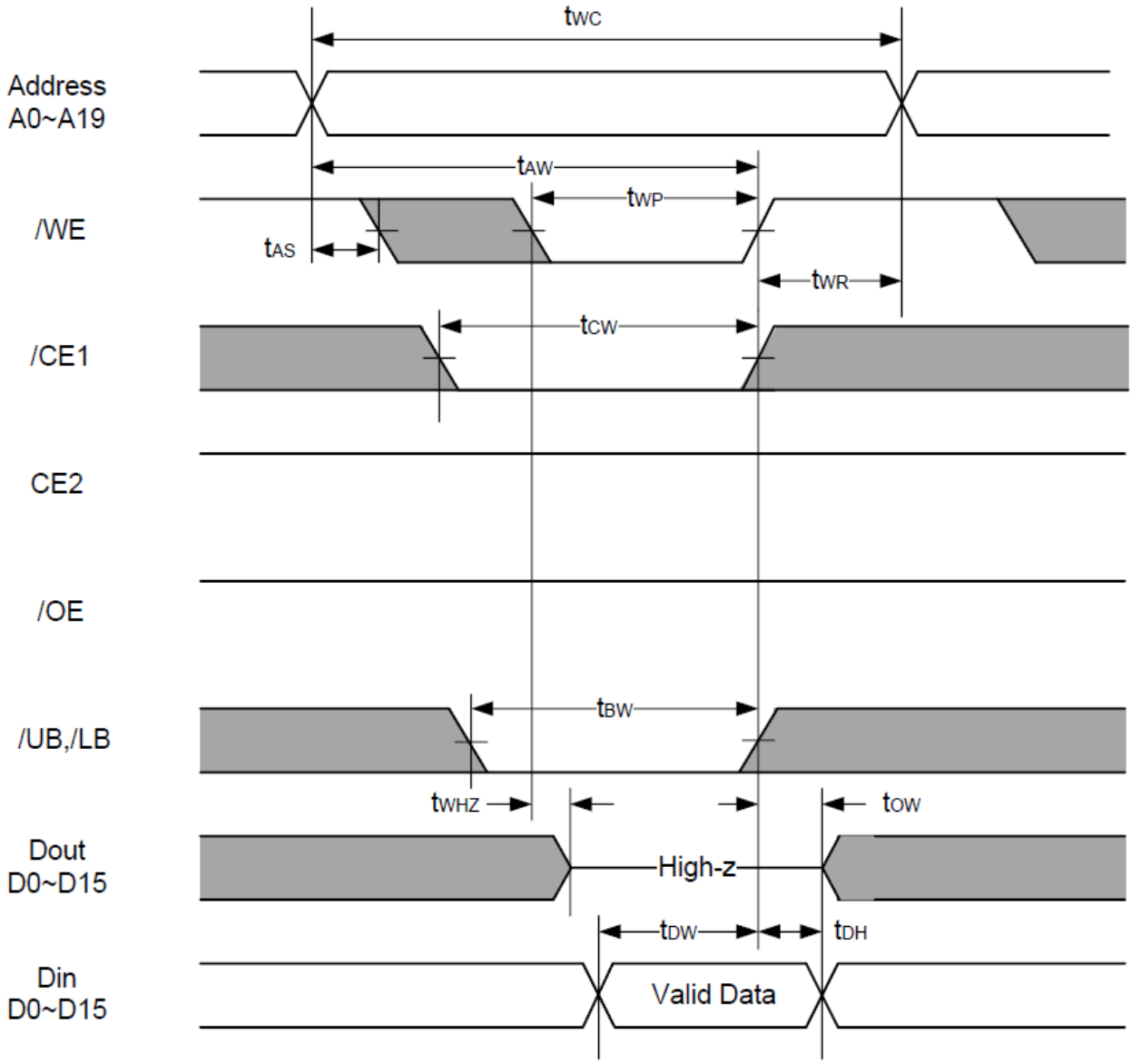
Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	120 (I_{SB1})	0
Deep Power Down	Invalid	15 (I_{SB0})	200

■ Timing Diagrams

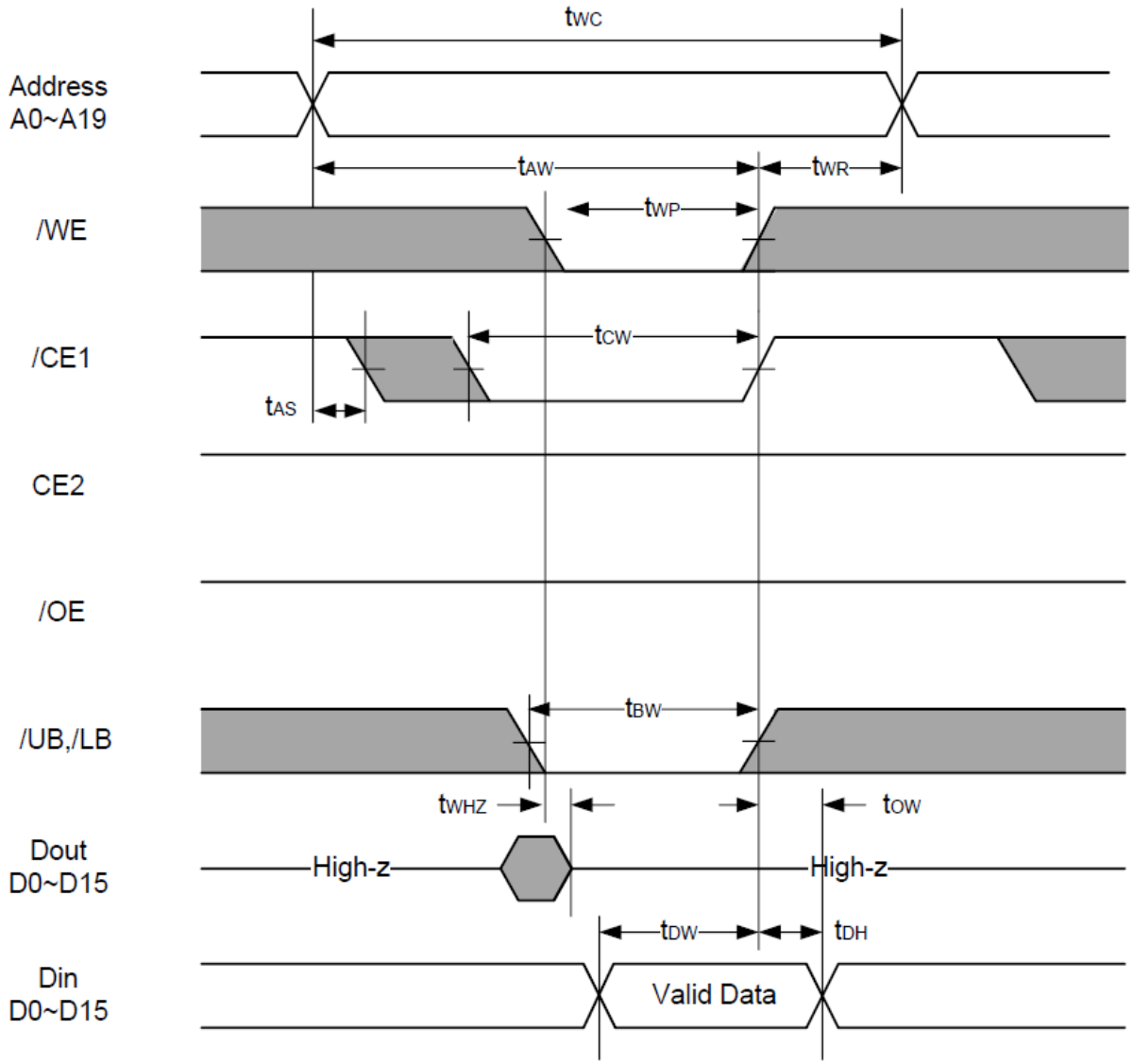
<Read Cycle>



Write Cycle (1) (/WE controlled)



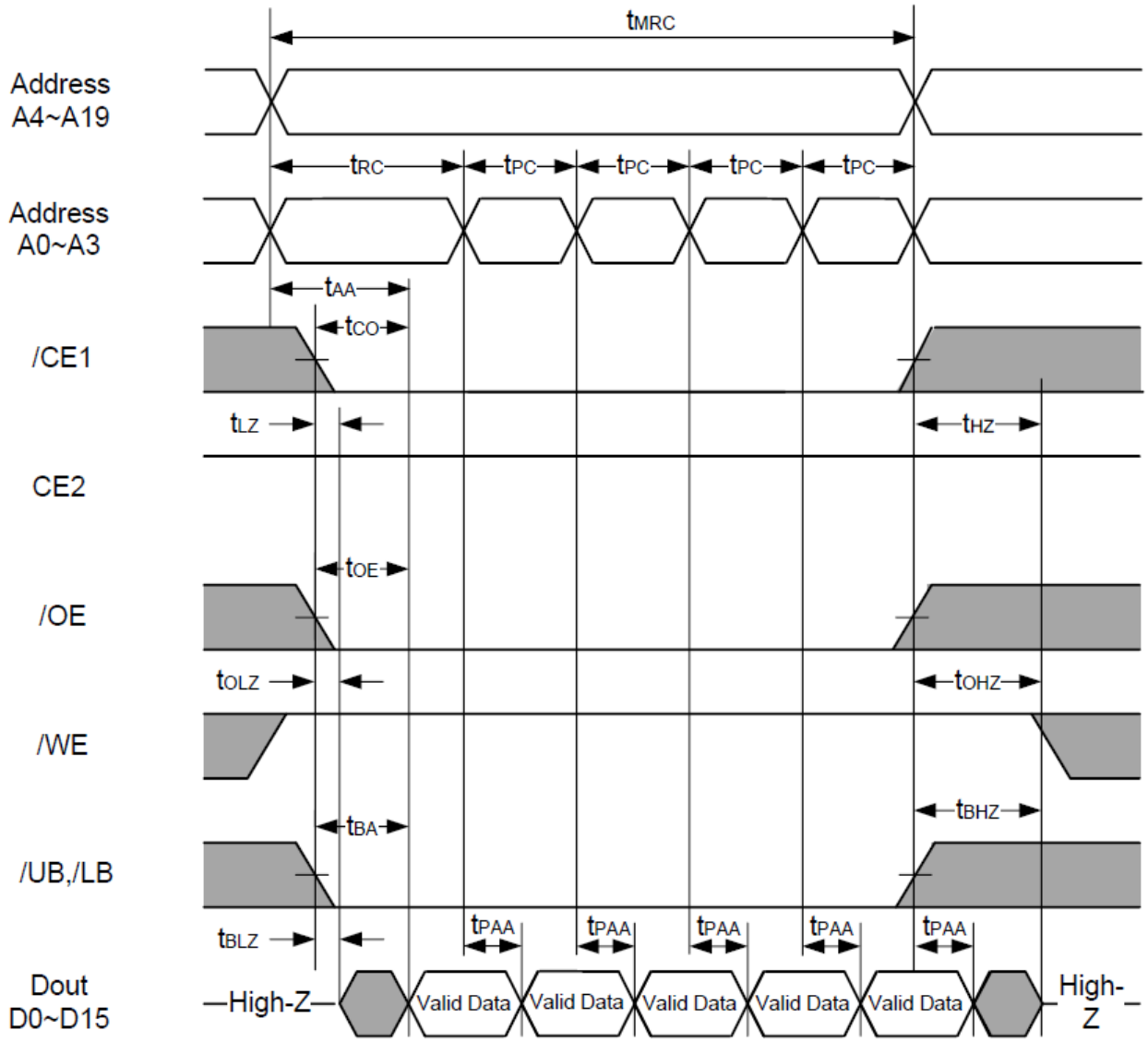
Write Cycle (2) (/CE1 controlled)



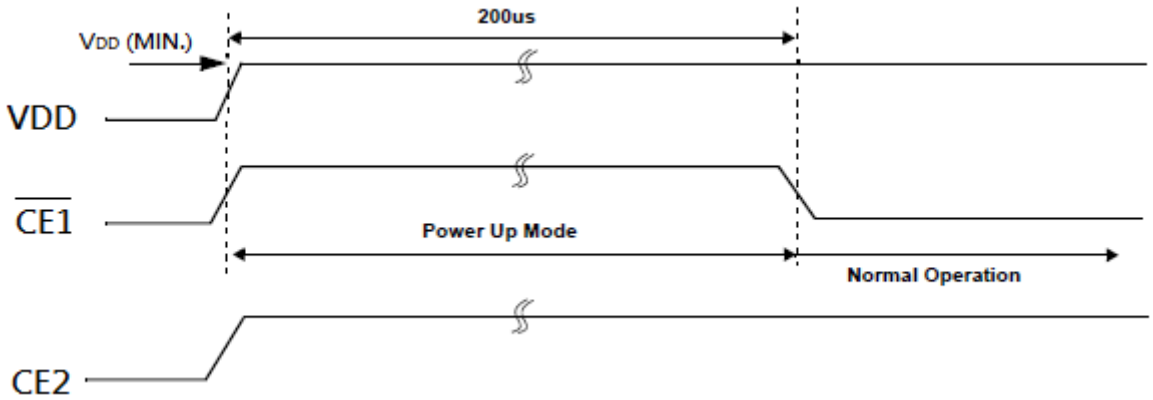
NOTES

1. AC measurement are assumed tR, tF = 5ns.
2. Parameters t_{HZ}、t_{OHZ}、t_{BHZ} and t_{WHZ} define the time at which the output goes the open condition and are not output voltage reference levels.
3. If /OE is high during the write cycle, the outputs will remain at high impedance.
4. During the output state of DQ signals, input signals of reverse polarity must not be applied.
5. If /CE1 or /LB&/UB goes LOW coincident with or after /WE goes LOW, the outputs will remain at high impedance.
6. If /CE1 or /LB&/UB goes HIGH coincident with or before /WE goes HIGH, the outputs will remain at high impedance.

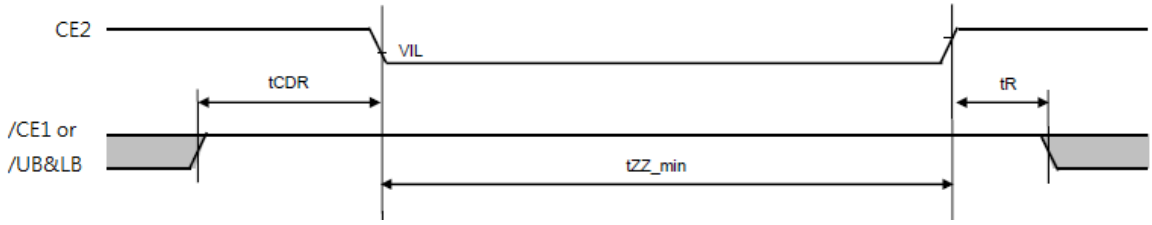
Page Read Cycle_16 Words Access



■ Power_On Timing



■ Deep Power Down Mode Entry/Exit



■ Order information

CS26LV16173X X X X XX

Version:
Blank: First Version
A: Second Version
..

Temperature:
C: 0~70°C
I: -40~85°C

Speed:
70: 70ns

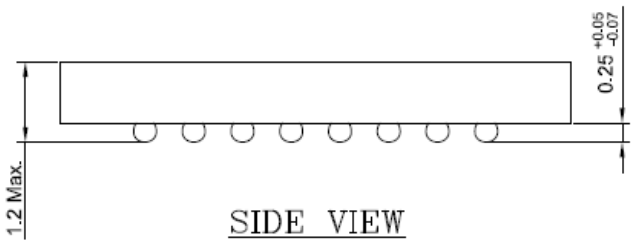
Package:
H: 48 ball TFBGA-6x8mm

Package Material:
-: Normal
P: Lead Free (TFBGA)

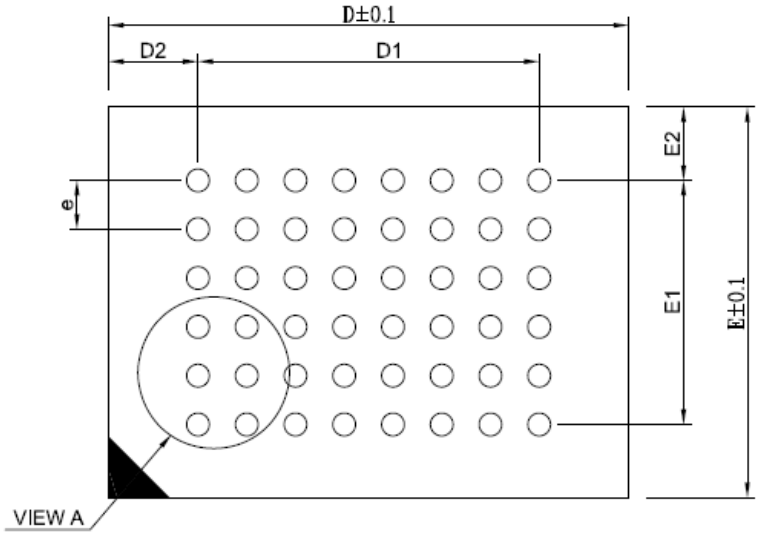
Note: Package material code “P” meets RoHS

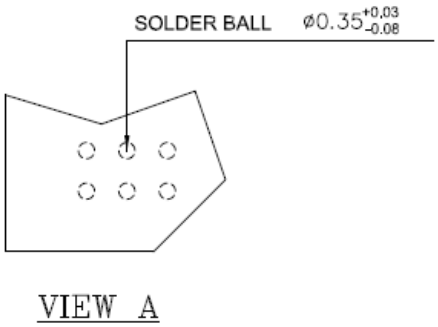
■ Package Dimensions:

48 ball TFBGA-6x8mm



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125





NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025