Revision History

Rev. No.	History	Issue Date	Remark
1.0	New Issue (65nm process)	May, 27, 2015	
2.0	Add test condition in AC Characteristics	Sep., 06, 2016	

Product Description

The CS26LV32163C is a 32M-bit PSRAM organized as 2Mwords by 16 bits. It provides high density, high speed andlow power. Thedevice also features SRAM-like W/R timing whereby thedevice is controlled by /CE, /OE and /WE on asynchronous.The device has the page access operation. Page size is16 words. The device also supports deep power-downmode, realizing low-power standby.The CS26LV32163C is available die form and 48-Ball TFBGA package.

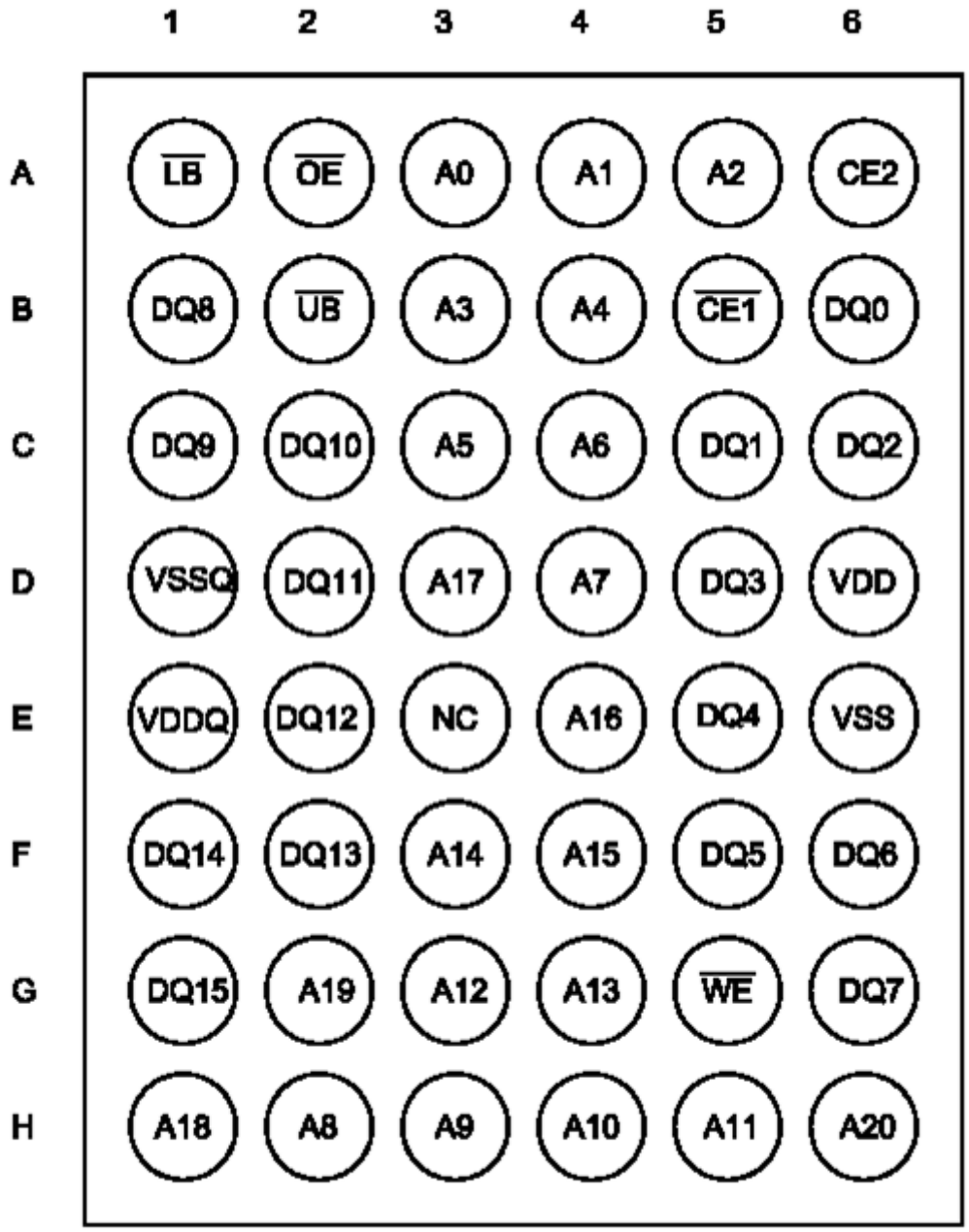
Features

- Single power supply voltage of 2.6 to 3.6V
- Direct TTL compatibility for all inputs and outputs.
- Deep power-down mode: Memory cell data invalid.
- Page operation mode
- Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  - Standby 120 uA(Max)
  - Deep power-down standby 20uA(Max.)
- Access Time
  - /CE1 Access Time: 70ns
  - /OE Access Time: 25ns
  - Page Access Time: 25ns

Product Family

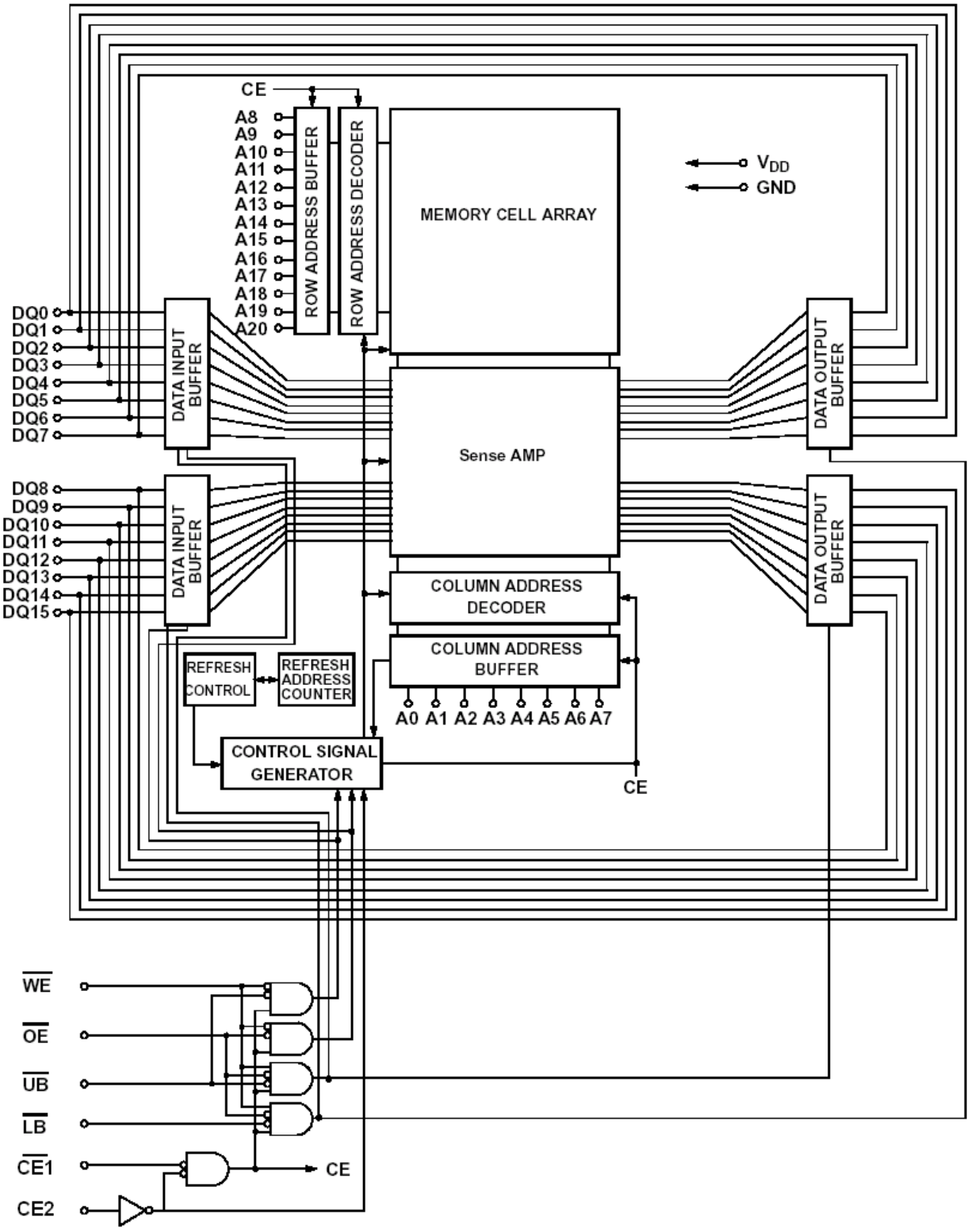
Part No.	Operating Temp	V_{DD}. Range	Speed	Standby (ISB, Max.)	Package Type
CS26LV32163C	0~70°C	2.6~3.6V	70ns	120uA	Dice 48 TFBGA-6x7mm
	-40~85°C			120uA	48 TFBGA-6x8mm

Pin Configuration



48 ball TFBGA- Top View

Functional Block Diagram



Pin Descriptions

Name	Type	Function
A0~A20	input	Address input
A0~A3	input	Page Address input
/CE1	input	Chip Enable Input1, Low : Enable
CE2	input	Chip Enable Input2, High: Enable, Low: Enter Power Down mode
/WE	input	Write Enable input, Low :Enable
/OE	input	Output Enable input, Low :Enable
/LB	input	Lower byte write control
/UB	input	Upper byte write control
DQ0~DQ15	I/O	Data inputs/outputs
V_{DD}	Power	Device Power supply
V_{SS}	Power	V_{SS}must be connected ground
V_{DDQ}	Power	I/O Power supply
V_{SSQ}	Power	V_{SSQ}must be connected ground
NC		Not Connection

Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V_{DD} Current
Deep power down	X	L	X	X	X	X	High Z	High Z	
Standby	H	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC}
Upper Byte Read					L	H	D_{OUT}	High Z	I_{CC}
Lower Byte Read					H	L	High Z	D_{OUT}	I_{CC}
Write	L	H	X	L	L	L	D_{IN}	D_{IN}	I_{CC}
Upper Byte Write					L	H	D_{IN}	Invalid	I_{CC}
Lower Byte Write					H	L	Invalid	D_{IN}	I_{CC}

Note: X means don't care. (Must be low or high state)

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{DD}	Voltage of V_{DD} supply relative to V_{SS}	-0.2 to V_{DDQ}+0.3	V
V_{IN}, V_{OUT}	Voltage at any pin relative to V_{SS}	-0.2 to V_{DDQ}+0.3	V
T_{STG}	Storage Temperature	-65 to +150	^{O}C
P_T	Power Dissipation	1.0	W

1. *Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

DC Electrical Characteristics (TA = -40 to + 85°C, V_{DD}= 2.6V~3.6V)

Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{IL}	Input Low Voltage (2)		-0.2		0.2*V_{DDQ}	V
V_{IH}	Input High Voltage (3)		0.8*V_{DDQ}		V_{DDQ}+0.2	V
I_{IL}	Input Leakage Current	V_{DD}=MAX, V_{IN}=V_{SS} to V_{DDQ}	-1		1	uA
I_{OL}	Output Leakage Current	V_{DD}=MAX, /CE1=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{DDQ}	-1		1	uA
V_{OL}	Output Low Voltage	V_{DD}=MAX, I_{OL} = 0.5mA			0.2*V_{DDQ}	V
V_{OH}	Output High Voltage	V_{DD}=MIN, I_{OH} = -0.5mA	0.8*V_{DDQ}			V
I_{CC1}	Operating Power Supply Current	Cycle time=1us, I_{IO}=0mA, 100% duty, /CE1≦0.2V, CE2≧ V_{DDQ}-0.2V, V_{IN}≦0.2V or V_{IN}≧V_{DDQ}-0.2V			5	mA
I_{CC2}		Cycle time=Min, I_{IO}=0mA, 100% duty, /CE1=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IL} or V_{IH}			25	mA
I_{CCSB1}	Standby Current -CMOS	/CE1 & CE2≧ V_{DDQ}-0.2V, V_{IN}≧ V_{DDQ}-0.2V or V_{IN}≦0.2V			120	uA
I_{CCSB2}	Deep Power-down Standby Current	CE2 < 0.2V, Other inputs = 0 ~ V_{DDQ} (Max. condition : V_{DD}=3.6V @ 85oC)			20	uA

1. *Typical characteristics are at TA = 25°C.*

2. *Undershoot: -1.0V in case of pulse width ≤20ns*
3. *Overshoot: VCC+ 1.0V in case of pulse width ≤20ns*
4. *Undershoot and overshoot are sampled, not 100% tested*

Capacitance (1) (T_A = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

1. *This parameter is sampled periodically and is not 100% tested*

AC Test Conditions

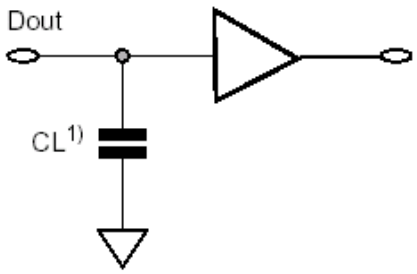
Test Conditions (Test Load and Test Input/output Reference)

Input Pulse Level : 0.2V to V_{DDQ}-0.2V

Input Rise and Fall Time : 5ns

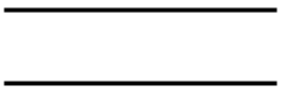
Input and Output reference Voltage : V_{DDQ} /2

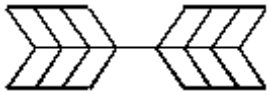
Output Load (See right) : $CL^{1)}$= 30pF



1. Including scope and Jig capacitance

Key to Switching Waveforms

Waveform	Inputs	Outputs
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don't care any change permitted	Change state unknown

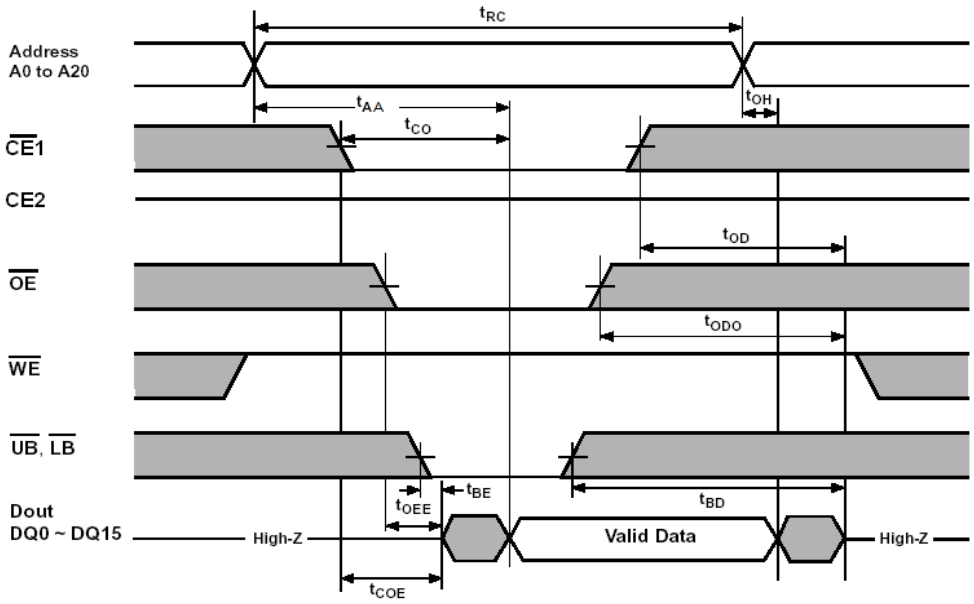
	Does not apply	Center line is high impedance “OFF” state

AC Characteristics<Read cycle& Write Cycle> (T_A = -40 to + 85ºC, V_{DD}= 2.6V~3.6V)

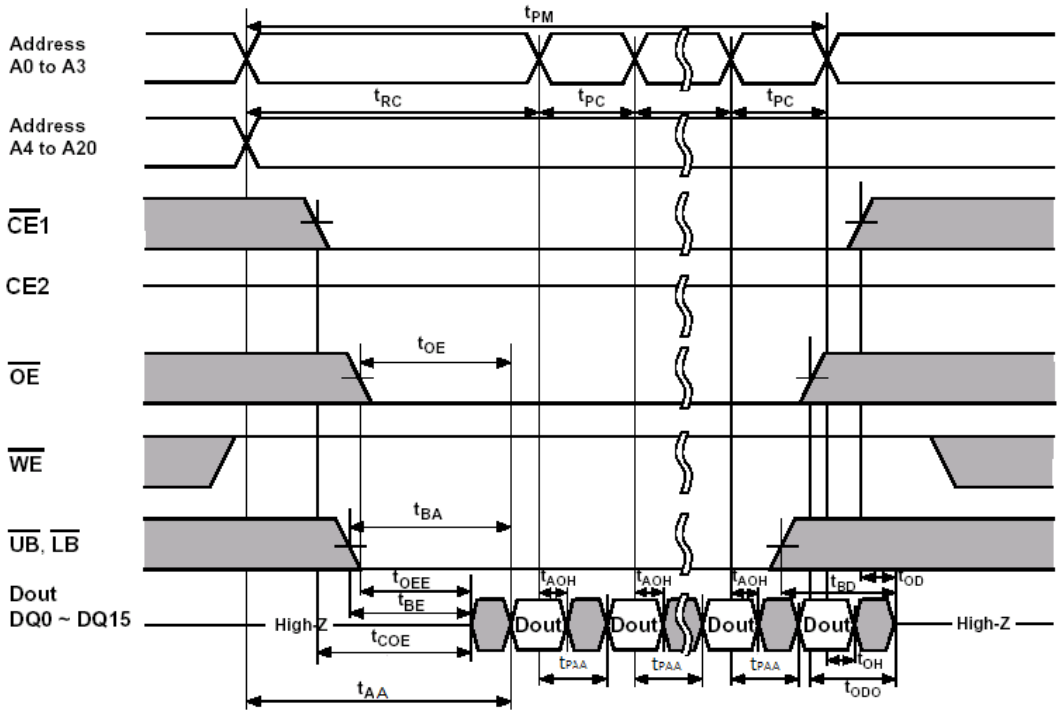
Parameter Name	Name	70		Unit
		Min	Max	
Read cycle time	t_{RC}	70	10,000	ns
Page mode Maximum cycle time	t_{MRC}	-	10,000	ns
Address access time	t_{AA}	-	70	ns
Page Address Access Time	T_{PAA}		25	ns
Chip enable access time (/CE1)	t_{CO}	-	70	ns
Output enable to output valid (/OE)	t_{OE}	-	25	ns
Byte enable access time	t_{BA}	-	25	ns
Output data hold time	t_{OH}	5	-	ns
Page mode output data hold time	t_{AOH}	-	25	ns
Chip enable to output in low Z (/CE1)	t_{COE}	10	-	ns
Output enable to output in low Z (/OE)	t_{OEE}	0	-	ns
Byte enable to output in low Z	t_{BE}	0	-	ns
Chip disable to output in High Z (/CE1)	t_{OD}	-	20	ns
Output disable to output in High Z (OE)	t_{ODO}	-	20	ns
Byte disable to output in High Z	t_{BD}	-	20	ns
Write cycle time	t_{WC}	70	10,000	ns
Byte enable to end of write	t_{BW}	60	-	ns
Address valid to end of write	t_{AW}	60	-	ns
Chip select to end of write	t_{CW}	60	-	ns
Data set up time	t_{DS}	20	-	ns
Data hold time	t_{DH}	0	-	ns
Write pulse width	t_{WP}	50	-	ns
Address set up time	t_{AS}	0	-	ns
Write recovery time(/WE)	t_{WR}	0	-	ns
/WE high to output low Z	t_{OEW}	0	-	ns
/WE low to output high Z	t_{ODW}	-	20	ns
Chip enable high pulse width	t_{CEH}	10		ns
Write enable high pulse width	t_{WEH}	6	-	ns
CE2 set –up time	t_{CS}	0	-	ns
CE2 hold time	t_{CH}	300	-	ns

CE2 pulse width	t_{DPD}	10	-	ns
CE2 hold from /CE1	t_{CHC}	0	-	ns
CE2 hold from power on	t_{CHP}	30	-	ns

TIMING DIAGRAMS<READ CYCLE>



PAGE READ CYCLE (16 words access)

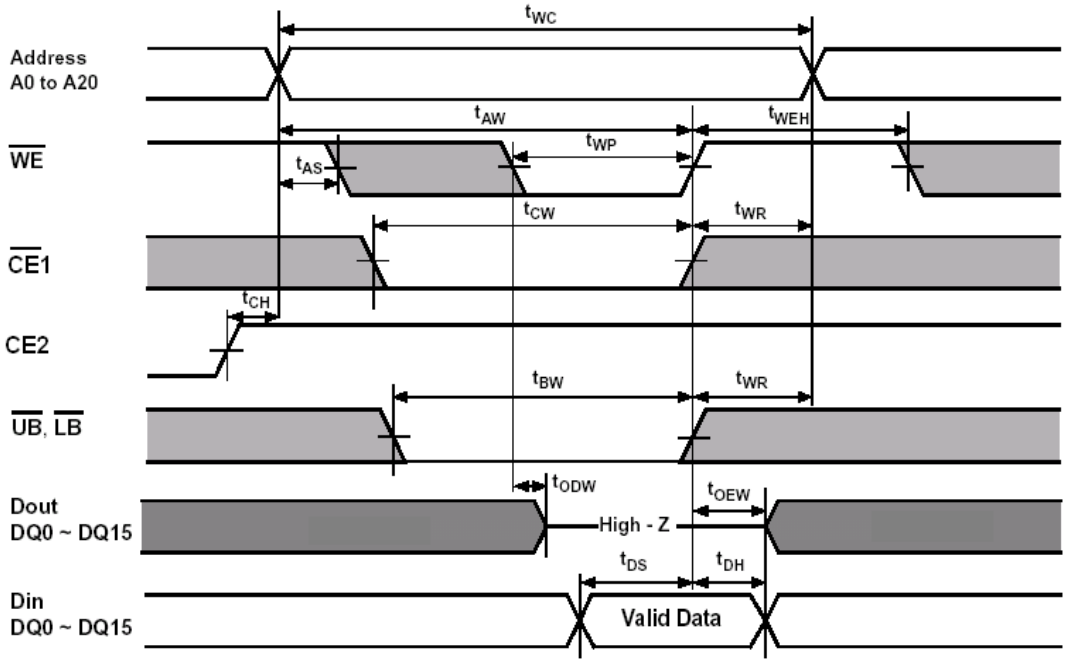


*(read cycle)

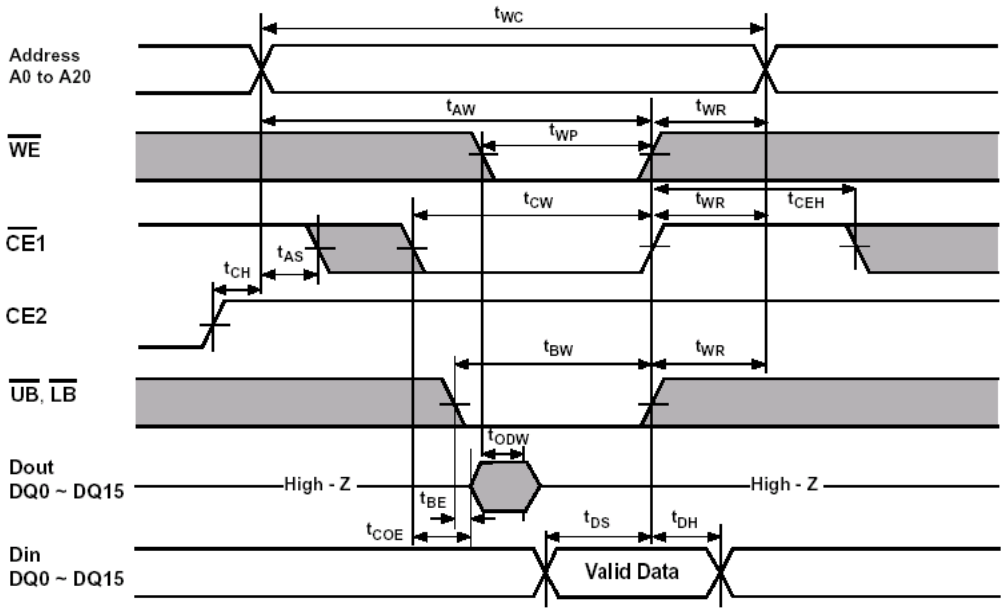
1. t_{HZ}, t_{BHZ}, t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not access device with cycle timing shorter than t_{RC} for continuous periods >10us

WRITE CYCLE (1) (/WE controlled)



WRITE CYCLE (2) (/CE1 controlled)



NOTES

1. AC measurement are assumed t_R, t_F = 5ns.

2. Parameters t_{OD}, t_{ODO}, t_{BD} and t_{ODW} define the time at which the output goes the open condition and are notoutput voltage reference levels.

3. Data cannot be retained at deep power-down stand-by mode.

4. If /OE is high during the write cycle, the outputs will remain at high impedance.

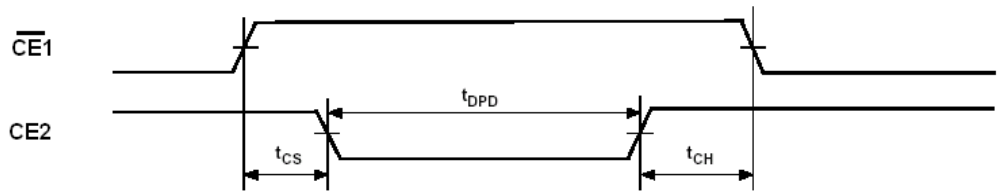
5. During the output state of DQ signals, input signals of reverse polarity must not be applied.

6. If /CE1 or /LB&/UB goes LOW coincident with or after /WE goes LOW, the outputs will remain at high impedance.

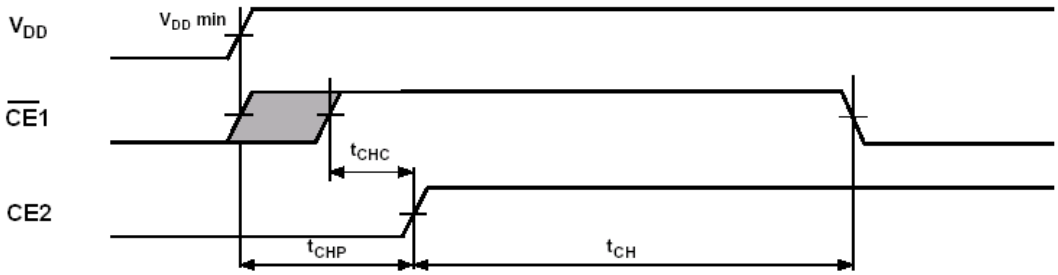
7. If /CE1 or /LB&/UB goes HIGH coincident with or before /WE goes HIGH, the outputs will remain at high impedance.

8. Do not access device with cycle timing shorter than t_{WC} for continuous periods > 10us.

DEEP POWER-DOWN TIMING



POWER_ON TIMING



Order Information

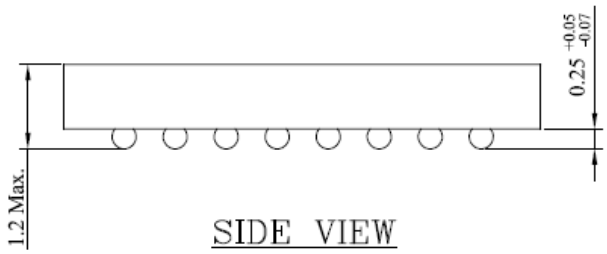
CS26LV32163C X X X XX

- Package: H: 48 ball TFBGA-6x8mm; Z: Dice
- Speed: 70: 70ns
- Temperature: C: 0~70°C; I: -40~85°C
- Package Material: - : Normal; P: Lead Free

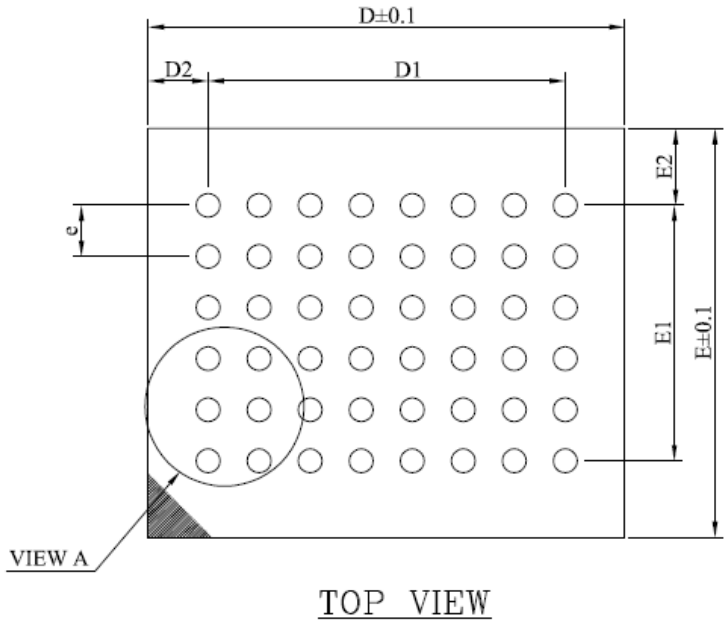
Note: Package material code "P" meets RoHS

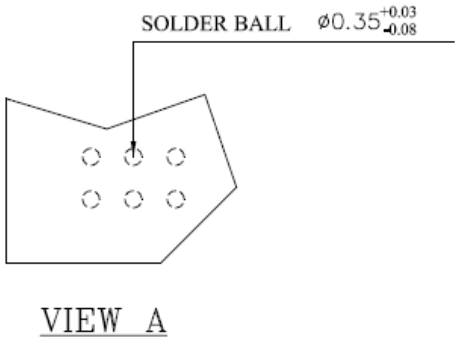
Package Outline

48 ball TFBGA-6x7mm



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
7.0	6.0	48	5.25	3.75	0.875	1.125

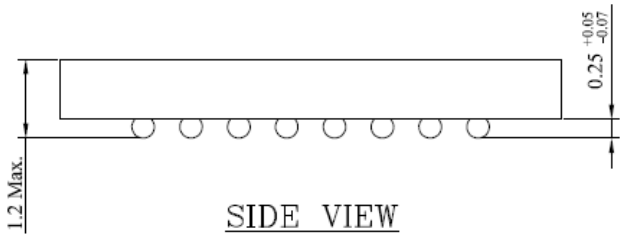




NOTES:

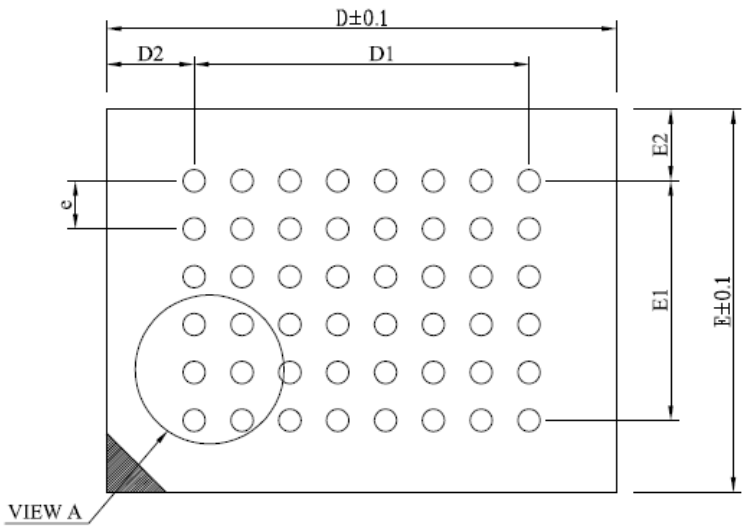
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025

48 ball TFBGA-6x8mm

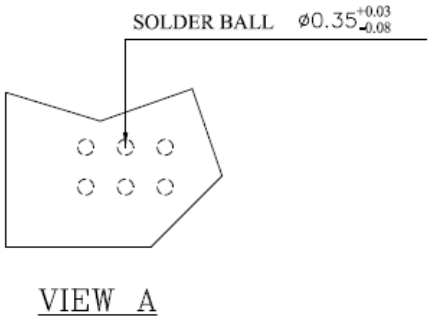


SIDE VIEW

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



TOP VIEW



VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025