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1. Product Description

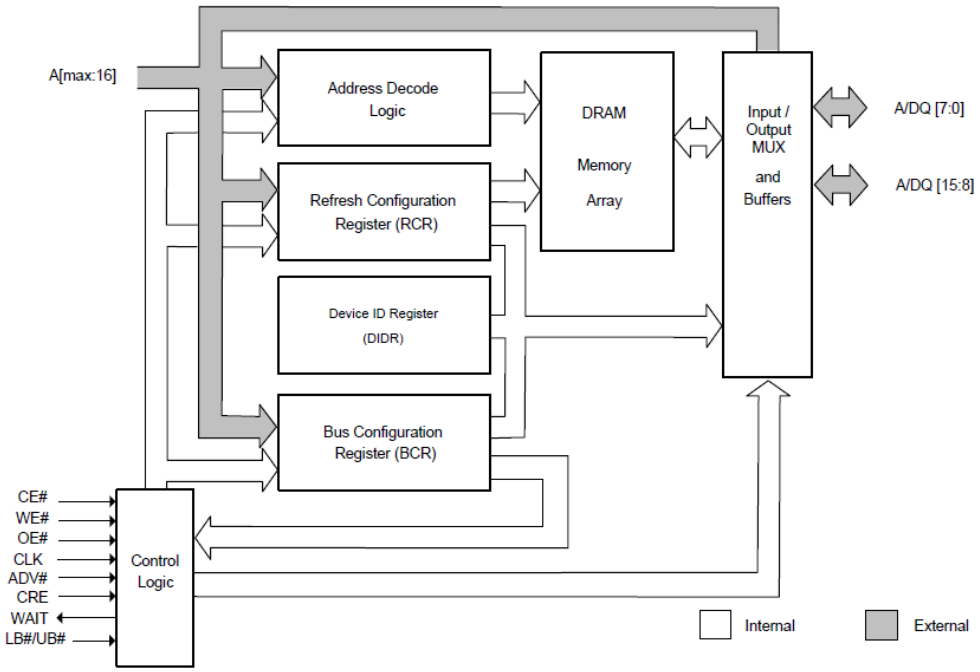
64M Cellular RAM products are high-speed, CMOS pseudo-static random-access memory developed for low-power, portable applications. The 64Mb Cellular RAM device has a DRAM core organized as 4 Meg x 16 bits. These devices are a variation of the industry-standard Flash control interface, with a multiplexed address/data bus. The multiplexed address and data functionality dramatically reduce the required signal count, and increases read/write bandwidth. For seamless operation on a burst Flash bus, 64M Cellular RAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance. Two user accessible control registers define device operation. The bus configuration register (BCR) defines how the 64M Cellular RAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation. Special attention has been focused on standby current consumption during self- refresh. 64M Cellular RAM products include two mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated self-refresh (TCSR) uses an on-chip sensor to adjust the refresh rate to match the device temperature-the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system configurable refresh mechanisms are accessed through the RCR. This 64M Cellular RAM specification defines the industry standard CellularRAM1.5 x16 A/D Mux feature set established by the Cellular RAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, a variety of wrap options, and a device ID register (DIDR).

2. Features

- Supports asynchronous, page, and burst operations
- VCC, VCCQ Voltages:
  - 1.7V–1.95V VCC
  - 1.7V–1.95V VCCQ
- Random access time: 70ns
- Burst mode READ and WRITE access:
  - 4, 8, 16, or 32 words, or continuous burst
  - Burst wrap or sequential
  - Max clock rate:
  - 133 MHz (tCLK = 7.5ns)
- Low power consumption:
  - Asynchronous random READ/WRITE: <25 mA
  - Continuous burst READ: <35 mA
  - Standby current: <250 µA
- Low-power features
  - On-chip temperature compensated refresh (TCR)
  - Partial array refresh (PAR)
  - Deep Power-Down (DPD) mode
- Configuration: 64Mb (4M x 16)
- 16-bit multiplexed address/data bus
- Support package:
  - 49 balls TFBGA (x16)
- Operating temperature range:
  - -40°C ≤ TCASE ≤ 85°C

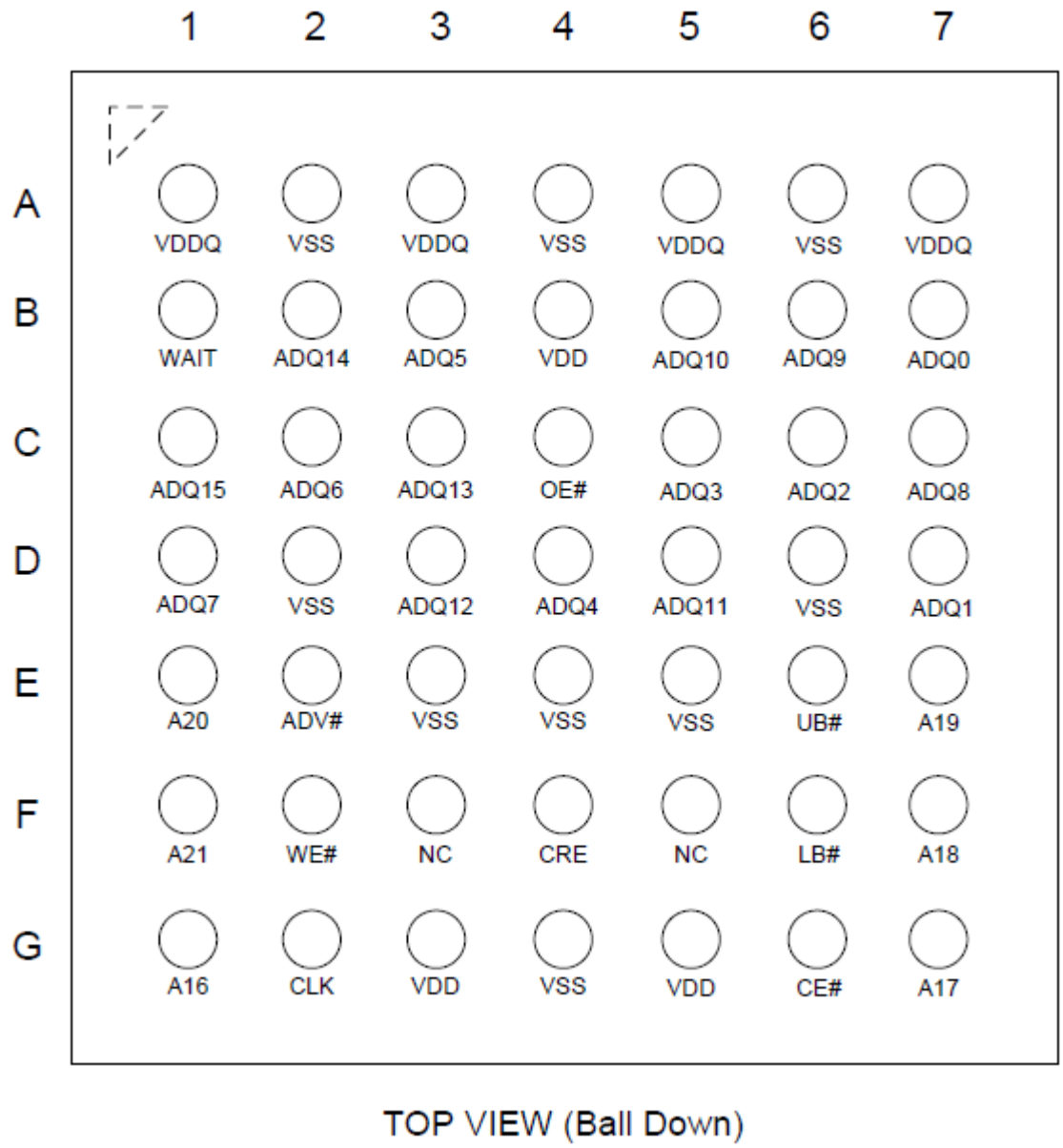
3. Functional Block Diagram

Fig 1: Functional Block Diagram



4. Ball Configuration

Fig 2 : Ball Configuration



TOP VIEW (Ball Down)

Table 1: Ball Description

Symbol	Type	Descriptions
A [21:16]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
CLK (note1)	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK must be static (HIGH or LOW) during asynchronous access READ and WRITE operations when burst mode is enabled.
ADV#	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses are latched on the rising edge of ADV# during asynchronous READ and WRITE operations.
CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
LB#	Input	Lower byte enables. DQ [7:0]
UB#	Input	Upper byte enables. DQ [15:8]
A/DQ [15:0]	Input/ Output	Address/data I/Os: These pins are a multiplexed address/data bus. As inputs for address, these pins behave as A [15:0]. A [0] is the LSB of the 16-bit word address within the Cellular RAM device. Address, RCR, and BCR values are loaded with ADV# LOW. Data is input or output when ADV# is HIGH.
WAIT (note1)	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is also asserted at the end of row unless wrapping within the burst length. Wait should be ignored during asynchronous operations. WAIT is High-Z when CE# is HIGH.
RFU	-	Reserved for future use.
VCC	Supply	Device power supply: (1.70V.1.95V) Power supply for device core operation.
VCCQ	Supply	I/O power supply: (1.70V.1.95V) Power supply for input/output buffers.
VSS	Supply	VSS must be connected to ground.
VSSQ	Supply	VSSQ must be connected to ground.

Note:

1. When using asynchronous mode exclusively, CLK can be tied to VSSQ or VCCQ. WAIT should be ignored during asynchronous mode operation*s.*

5. INSTRUCTION SET

Table 2: Bus Operation

Asynchronous Mode BCR[15]=1	Power	CLK	ADV#	CE#	OE#	WE#	CRE	UB#/ LB#	WAIT2	A/DQ[15:0]	Notes
Read	Active	X	⌐¬	L	L	H	L	L	Low-z	Data out	4
Write	Active	X	⌐¬	L	X	L	L	L	High-z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-z	High-z	5, 6
No operation	Idle	X	X	L	X	X	L	X	Low-z	X	4, 6
Configuration register write	Active	X	⌐¬	L	H	L	H	X	Low-z	High-z	
Configuration register read	Active	X	⌐¬	L	L	H	H	L	Low-z	Config. Reg.out	
DPD	Deep Power-down	L	X	H	X	X	X	X	High-z	High-z	7
Burst Mode BCR[15]=0	**Power**	**CLK**	**ADV#**	**CE#**	**OE#**	**WE#**	**CRE**	**UB#/ LB#**	**WAIT**	**A/DQ[15:0]**	**Notes**
Async read	Active	H or L	⌐¬	L	L	H	L	L	Low-z	Data out	4, 8
Async write	Active	H or L	⌐¬	L	X	L	L	L	High-z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-z	High-z	5, 6
No operation	Idle	H or L	X	L	X	X	L	X	Low-z	X	4, 6
Initial burst read	Active	⌐¬	L	L	X	H	L	L	Low-z	Address	4, 9
Initial burst write	Active	⌐¬	L	L	H	L	L	X	Low-z	Address	4, 9
Burst continue	Active	⌐¬	H	L	X	X	X	L	Low-z	Data out or Data in	4, 9
Configuration register write	Active	⌐¬	L	L	H	L	H	X	Low-z	High-z	9, 10
Configuration register read	Active	⌐¬	L	L	L	H	H	L	Low-z	Config. Reg.out	9, 10
DPD	Deep Power-down	L	X	H	X	X	X	X	High-z	High-z	7

Notes:

1. With burst mode enabled, CLK must be static (LOW) during asynchronous READs and asynchronous WRITEs and to achieve standby power during standby and DPD modes.

2. The WAIT polarity is configured through the bus configuration register (BCR [10]).

3. When LB# and UB# are in select mode (LOW), DQ [15:0] are enabled. When only LB# is in select mode, DQ [7:0] are

enabled. When only UB# is in the select mode, DQ [15:8] are enabled.

4. The device will consume active power in this mode whenever addresses are changed.

5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.

6. VIN = VCCQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.

7. When the BCR is configured for synchronous mode, synchronous READ and WRITE and asynchronous WRITE and READ are supported.

8. Burst mode operation is initialized through the bus configuration register (BCR [15])

9. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single word burst (as indicated by WAIT).

10. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR [4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.

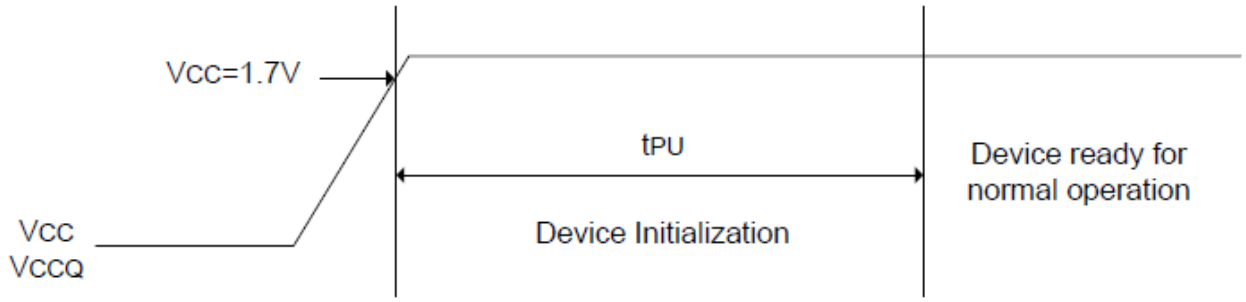
FUNTIONAL DESCRIPTION

In general, 64M Cellular RAM devices are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The 64Mb device contains a 67,108,864-bit DRAM core, organized as 4,194,304 addresses by 16 bits. The device implements a multiplexed address/data bus. This multiplexed configuration supports greater bandwidth through the x16 data bus, yet still reduces the required signal count. The 64M Cellular RAM bus interface supports both asynchronous and burst mode transfers.

POWER-UP INITIALIZATION

64M Cellular RAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings. VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150μs to complete its self-initialization process. Until the end of ^{t}PU, CE# should track VccQ and remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 2: Power-Up Initialization Timing



BUS OPERATING MODES

64M Cellular RAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR.

Asynchronous Mode

Asynchronous mode uses the industry- standard SRAM control signals (CE#, ADV#, OE#, WE#, and LB#/UB#). READ operations (Figure 3 on page 11) are initiated by bringing CE#, ADV#, and LB#/UB# LOW while keeping OE# and WE# HIGH and driving the address onto the A/DQ bus. ADV# is taken HIGH to capture the address, and OE# is taken LOW. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 4 on page 11) occur when CE#, ADV#, WE#, and LB#/UB# are driven LOW. with the address on the A/DQ bus. ADV# is taken HIGH to capture the address, then the WRITE data is driven onto the bus. During asynchronous WRITE operations, the OE# level is a “Don't Care,” and WE# will override OE#; however, OE# must be HIGH while the address is driven onto the A/DQ bus. The data to be written is latched on the rising edge of CE#, WE#, UB#, or LB# (whichever occurs first). During asynchronous operations with burst mode enabled, the CLK input must be held static (HIGH or LOW). WAIT will be driven during asynchronous READs, and its state should be ignored. WE# LOW time must be limited to tCEM.

Figure 3: READ Operation

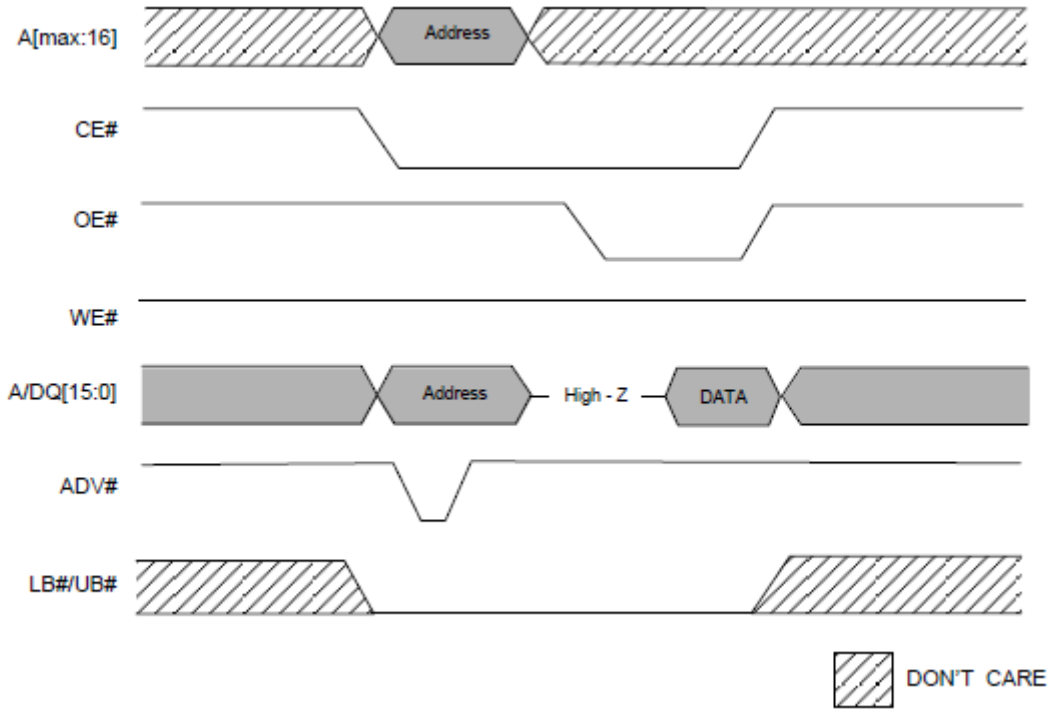
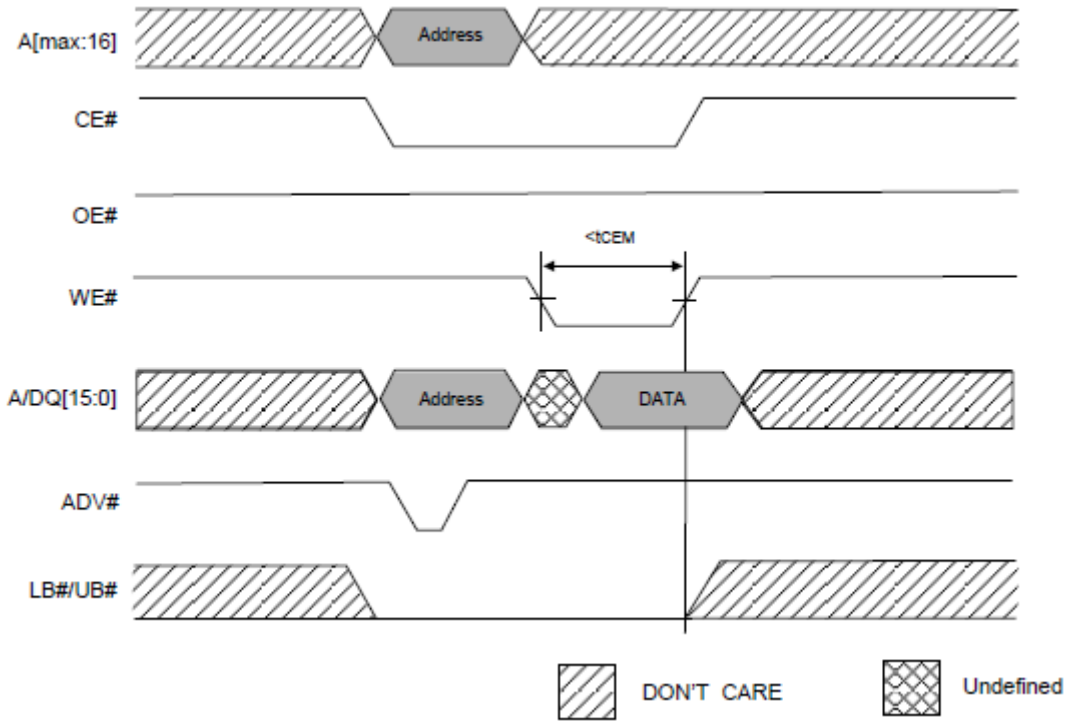


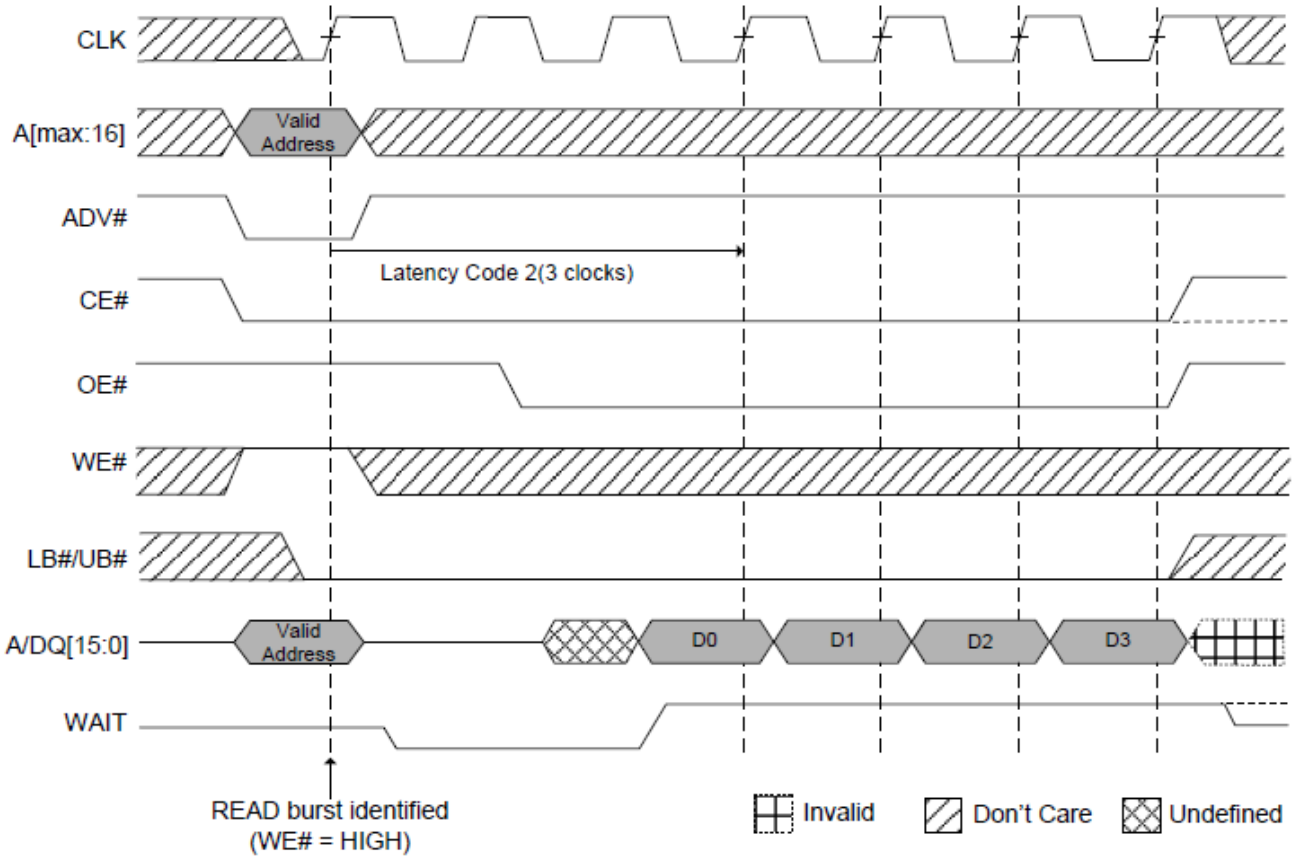
Figure 4: WRITE Operation



Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the rising edge of the next clock that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 5) or WRITE (WE# = LOW, Figure 6 on page 13).

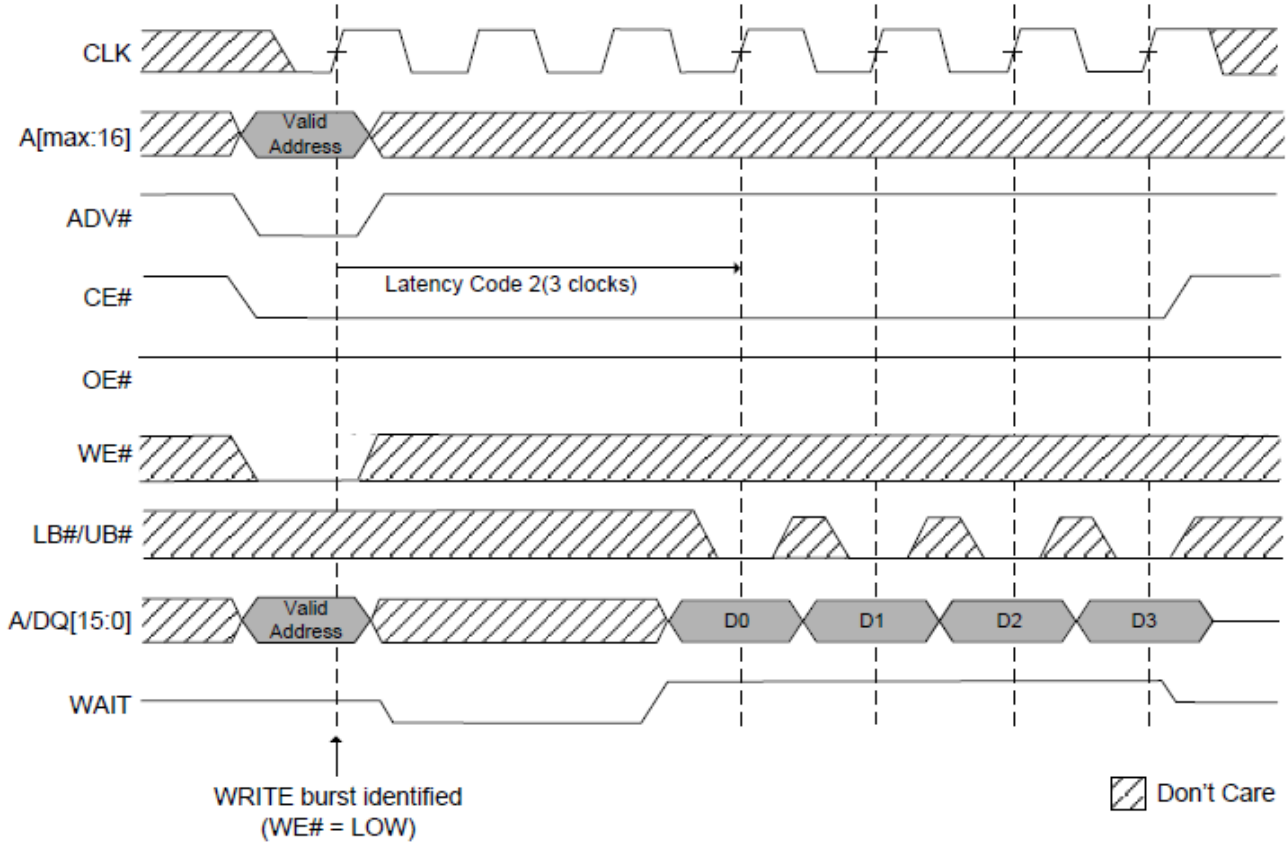
Figure 5: Burst Mode READ (4-word burst)



Note:

Non-default BCR settings for burst mode READ (4-word burst): fixed or variable latency, Latency code 2 (3 clocks), WAIT active Low, WAIT asserted during delay. Diagram is representative of variable latency with no refresh collision or fixed-latency access.

Figure 6: Burst Mode WRITE (4-word burst, OE# HIGH)



Note:

Non-default BCR settings for burst mode WRITE (4-word burst): fixed or variable latency, latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. Continuous bursts have the ability to start at a specified address and burst to the end of the address. It goes back to the first address and continues to burst when continuous bursts meet the end of address.

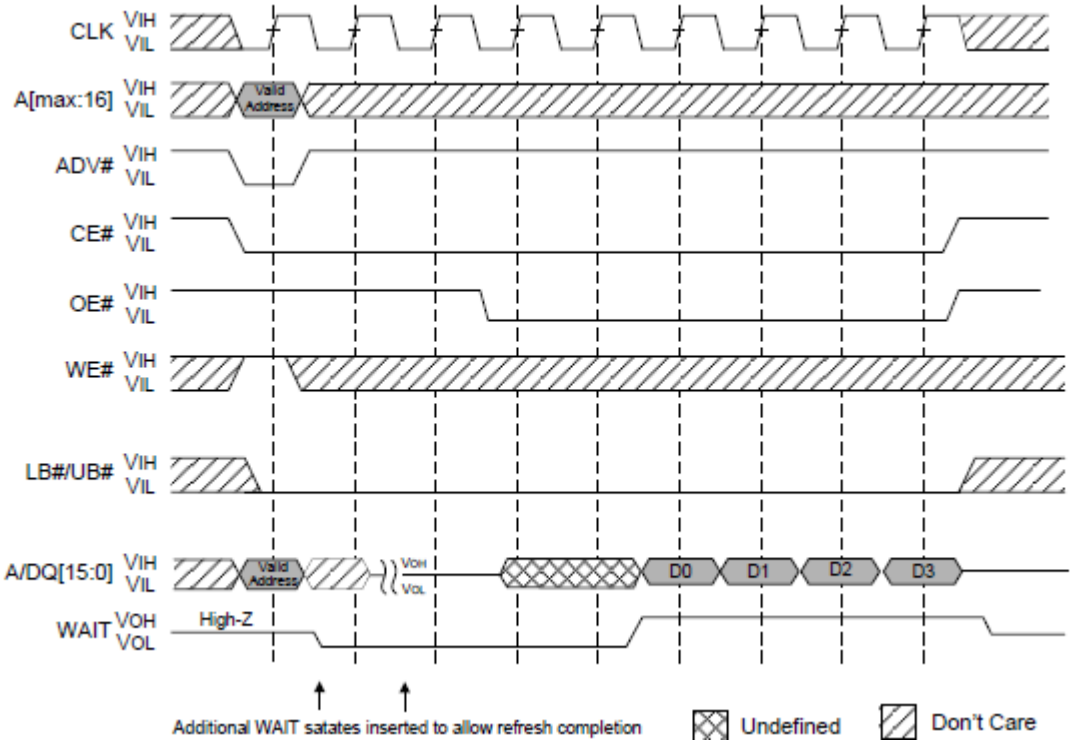
The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and Cellular RAM device. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows the Cellular RAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles.

Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

The WAIT output asserts when a burst is initiated, and de-asserts to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted at the boundary of the row, unless wrapping within the burst length. With wrap off, the Cellular RAM device will restore the previous row's data and access the next row, WAIT will be de-asserted, and the burst can continue across the row boundary(See Figure 29 on page 42 for a READ, Figure 34 on page 47 for a WRITE). If the burst is to terminate at the row boundary, CE# must go HIGH within 2 clocks of the last data (See Figure 28 on page 41). CE# must go HIGH before any clock edge following the last word of a defined-length burst WRITE (See Figure 31 and 32 on pages 44 and 45).

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM}. If a burst suspension will cause CE# to remain LOW for longer than t_{CEM}, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

Figure 7: Refresh Collision During Variable-Latency READ Operation



Note:
Non-default BCR settings for refresh collision during variable-latency READ operation: latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.

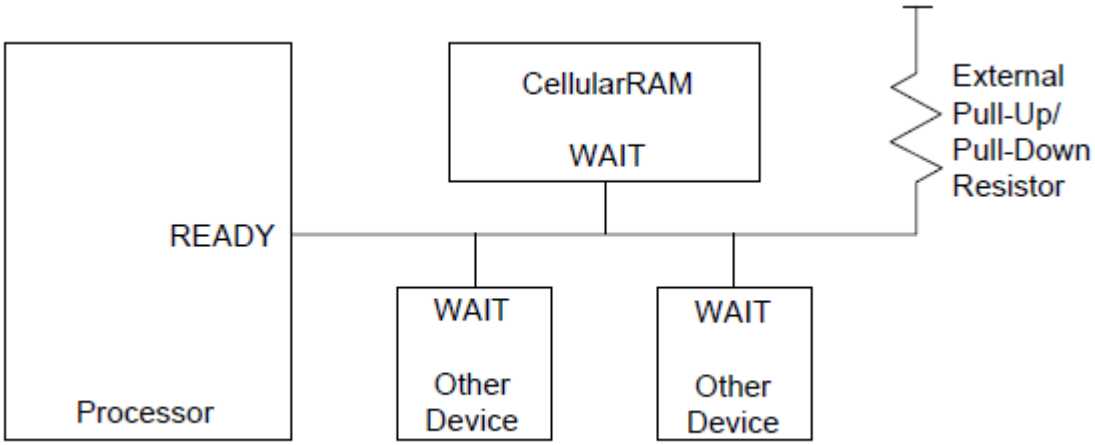
Mixed-Mode Operation

The device supports a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous WRITE operations require that the clock (CLK) remain static (HIGH or LOW) during the entire sequence. The ADV# signal can be used to latch the target address. CE# can remain LOW when the device is transitioning between mixed-mode operations with fixed latency enabled; however, the CE# LOW time must not exceed tCEM. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 37 on page 50 for the “Asynchronous WRITE Followed by Burst READ” timing diagram.

WAIT Operation

The WAIT output on a Cellular RAM device is typically connected to a shared, system-level WAIT signal (See Figure 8). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 8: Wired or WAIT Configuration



When a burst READ or WRITE operation has been initiated, WAIT goes active to indicate that the Cellular RAM device requires additional time before data can be transferred. For burst READ operations, WAIT will remain active until valid data is output from the device. For burst WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the Cellular RAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during this initial latency may cause data corruption.

When using variable initial access latency (BCR [14] = 0), the WAIT output performs an arbitration role for burst READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed (See Figure 7 on page 14). When the refresh operation has completed, the burst READ operation will continue normally.

WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed.

WAIT will be asserted after OE# goes LOW during asynchronous READ operations. WAIT will be High-Z during asynchronous WRITE operations. WAIT should be ignored during all asynchronous operations.

By using fixed initial latency (BCR [14] = 1), this Cellular RAM device can be used in burst mode without monitoring the WAIT signal. How- ever, WAIT can still be used to determine when valid data is available at the start of the burst and at the end of the row. If WAIT is not monitored, the controller must properly terminate all burst accesses at row boundaries on its own.

LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB# and UB# must be LOW during READ cycles. When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

LOW-POWER OPERATION

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH. The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh

Temperature compensated self-refresh (TCSR) allows for adequate refresh at different temperatures. This Cellular RAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually monitors the temperature to select an appropriate self-refresh rate.

Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (See Table 7 on page 29). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the Cellular RAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re- enabled, the Cellular RAM device will require 150μs to perform an initialization procedure before normal operations can resume. During this 150μs period, the current consumption will be higher than the specified

standby levels, but considerably lower than the active current specification. DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when CE# goes HIGH. DPD is disabled the next time CE# goes LOW and stays LOW for at least 10μs.

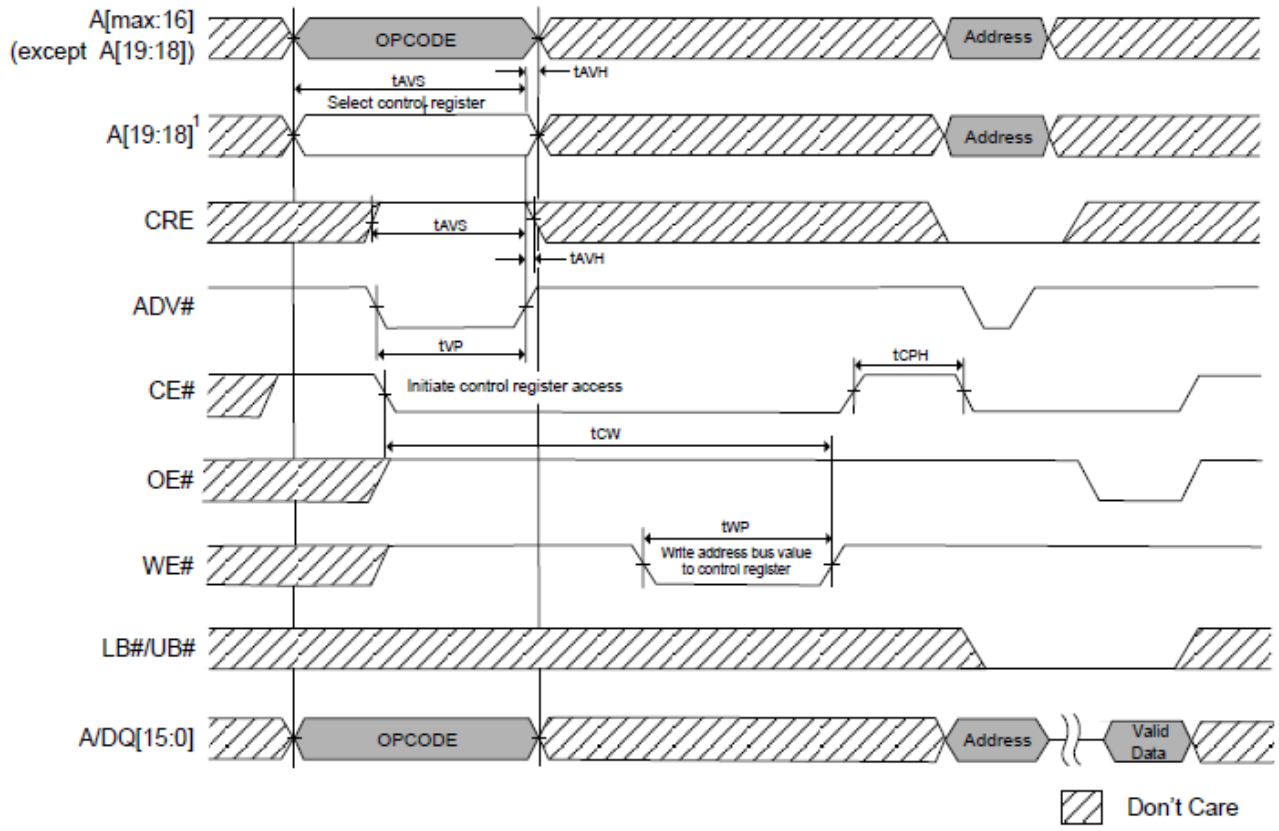
Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the Cellular- RAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time the devices are operating in a standby state. A DIDR provides information on the device manufacturer, Cellular RAM generation, and the specific device configuration. The DIDR is read-only.

Access Using CRE

The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH (see Figure 9 through 12 on pages 17 through 20). When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A [21:16] and A/DQ [15:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of CE# or WE#, whichever occurs first; LB# and UB# are “Don’t Care”. The BCR is accessed when A [19:18] are 10b; the RCR is accessed when A [19:18] are 00b. The DIDR is read when A [19:18] are 01b. For READs, address inputs other than A [19:18] are “Don’t Care” and register bits 15:0 are output on DQ [15:0]. Immediately after a configuration register READ or WRITE operation is performed, reading the memory array is highly recommended.

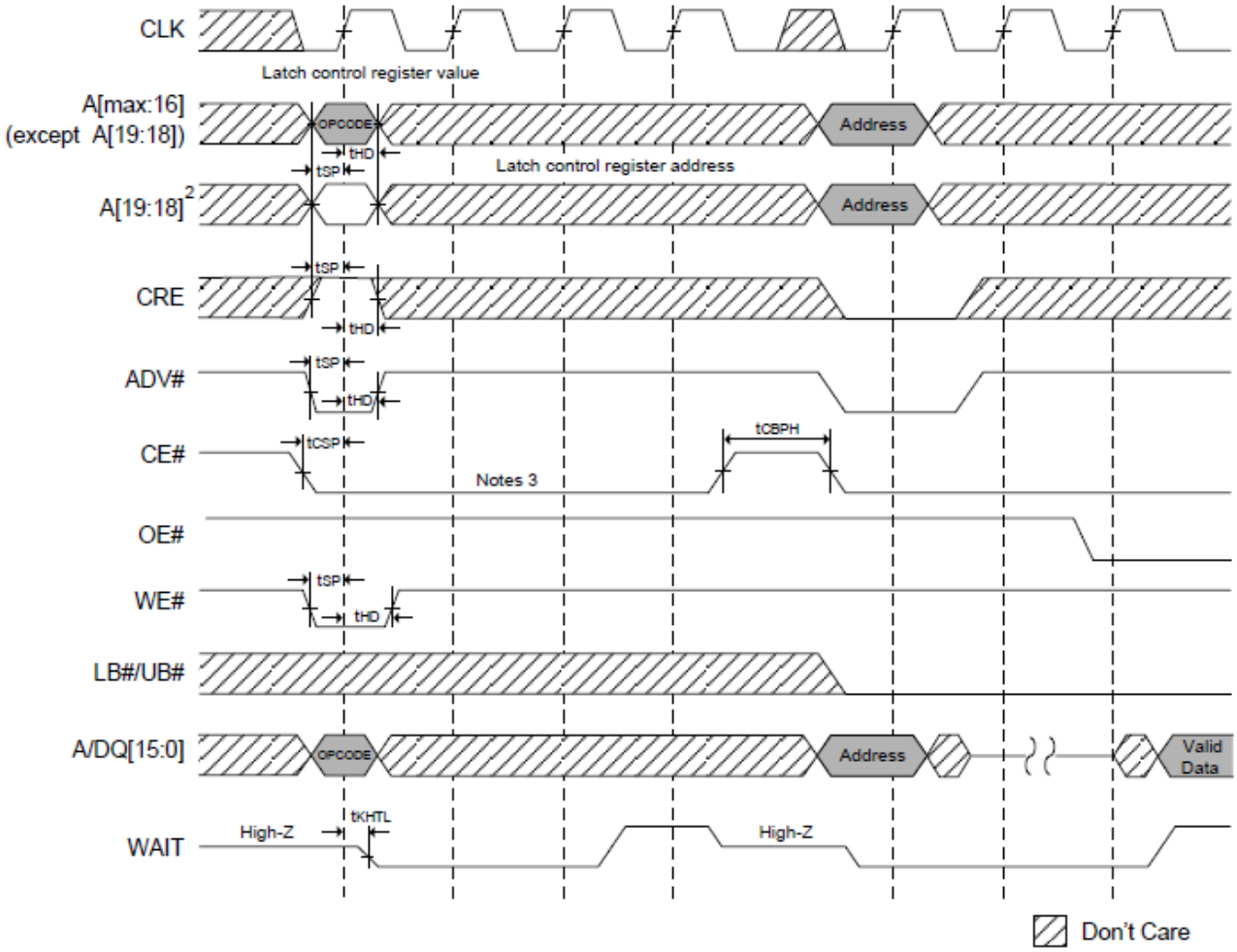
Figure 9: Configuration Register WRITE, Asynchronous Mode, Followed by READ ARRAY Operation



Note:

1. A [19:18] = 00b to load RCR, and 10b to load BCR.

Figure 10: Configuration Register WRITE, Synchronous Mode, Followed by READ ARRAY Operation



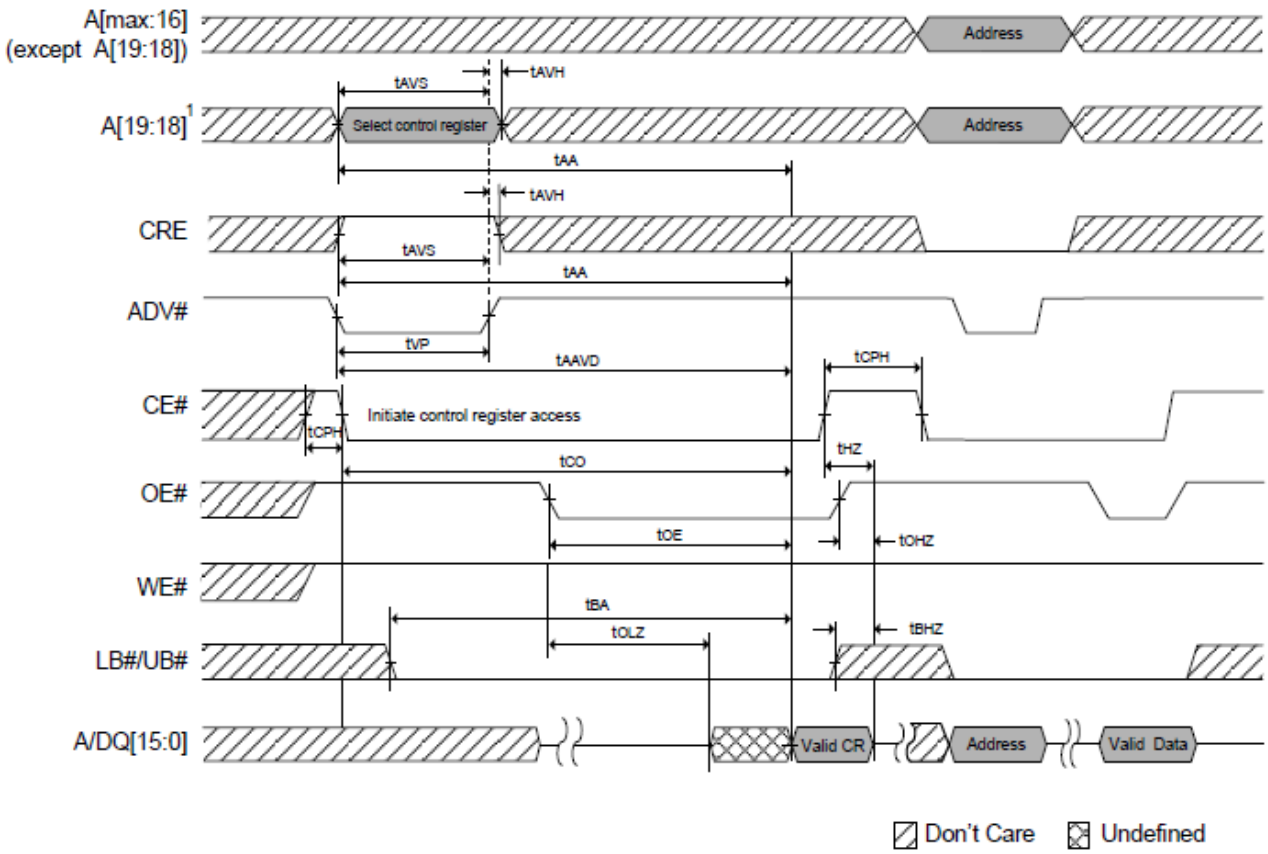
Notes:

1. Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.

2. A [19:18] = 00b to load RCR, and 10b to load BCR.

3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

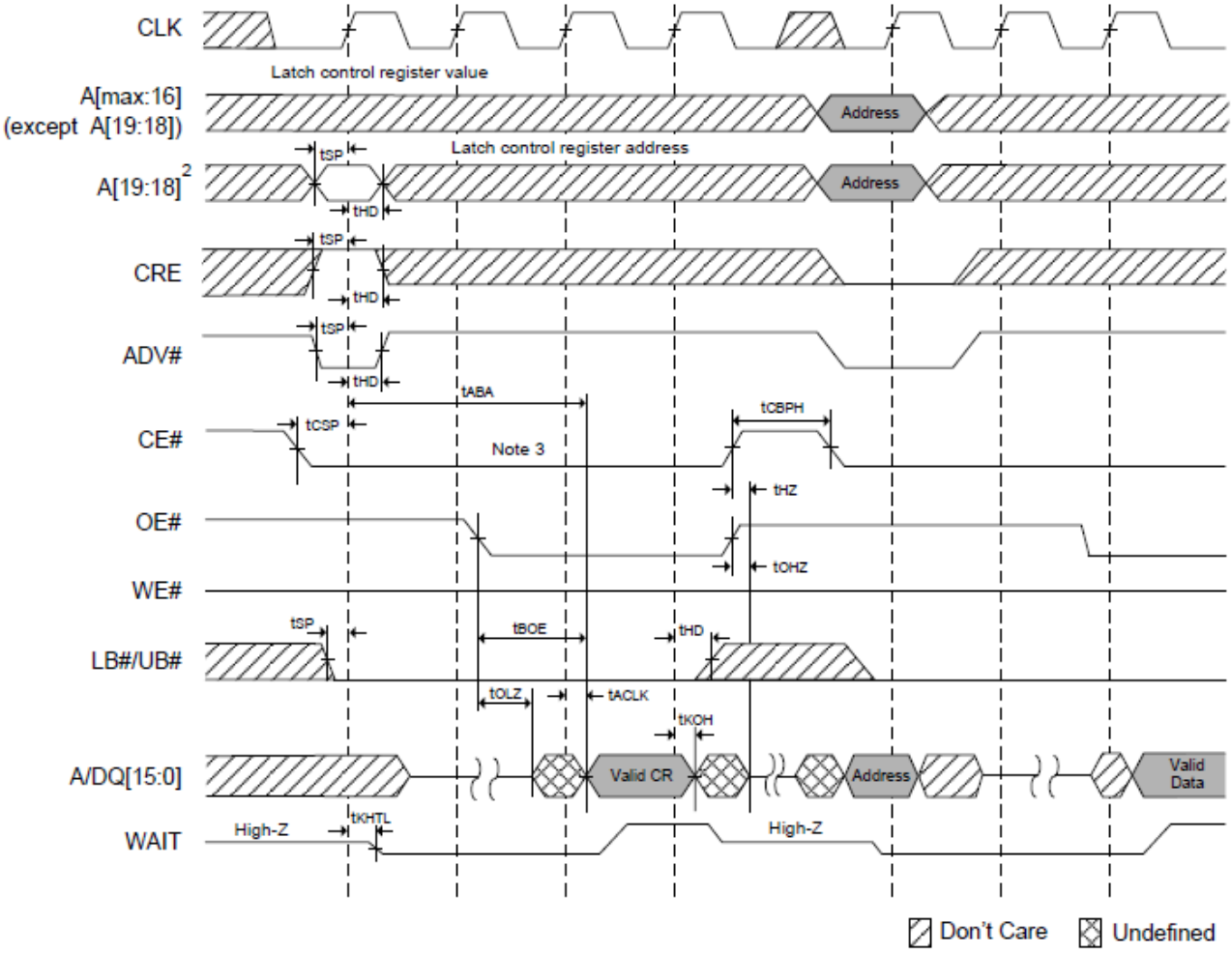
Figure 11: Register READ, Asynchronous Mode, Followed by READ ARRAY Operation



Note:

A [19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

Figure 12: Register READ, Synchronous Mode, Followed by READ ARRAY Operation



Notes:

1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code 2 (3 clocks): WAIT active LOW; WAIT asserted during delay.
2. A [19:18] =00b to read RCR,10b to read BCR, and 01b to read DIDR.
3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Software Access

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified, and all registers can be read using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 13). The READ sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 14). The address used during all READ and WRITE operations is the highest address of the Cellular RAM device being accessed (3FFFFFh); the contents of this address are not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ [15:0] transfer data in to or out of bits 15:0 of the registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

Figure 13: Load Configuration Register

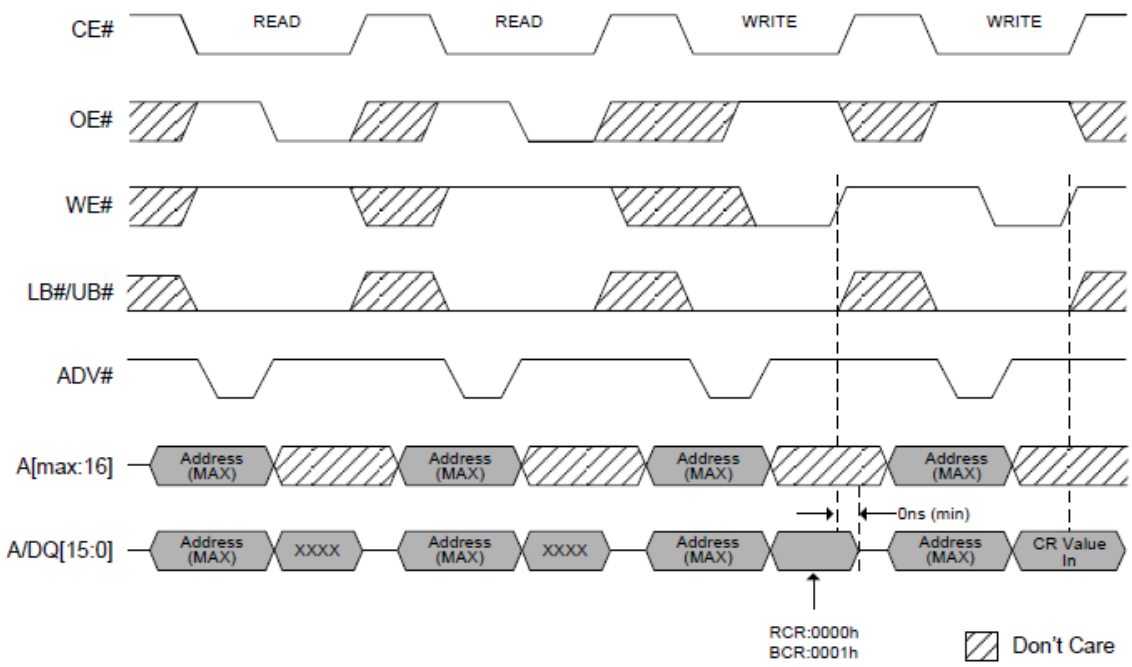
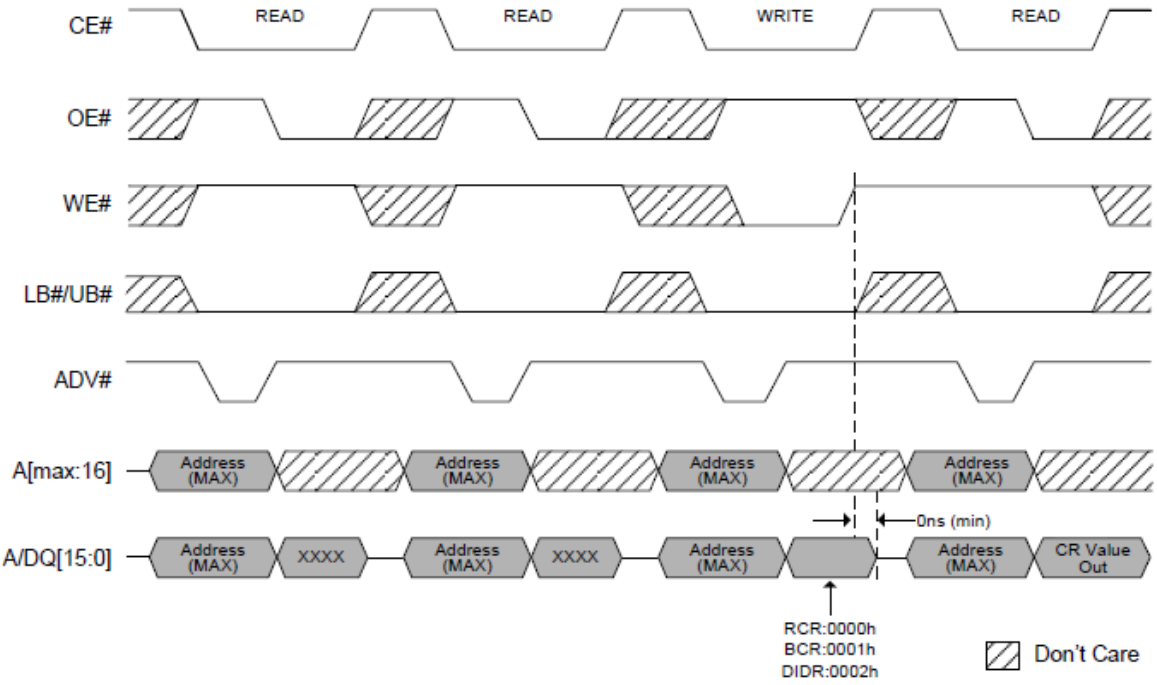


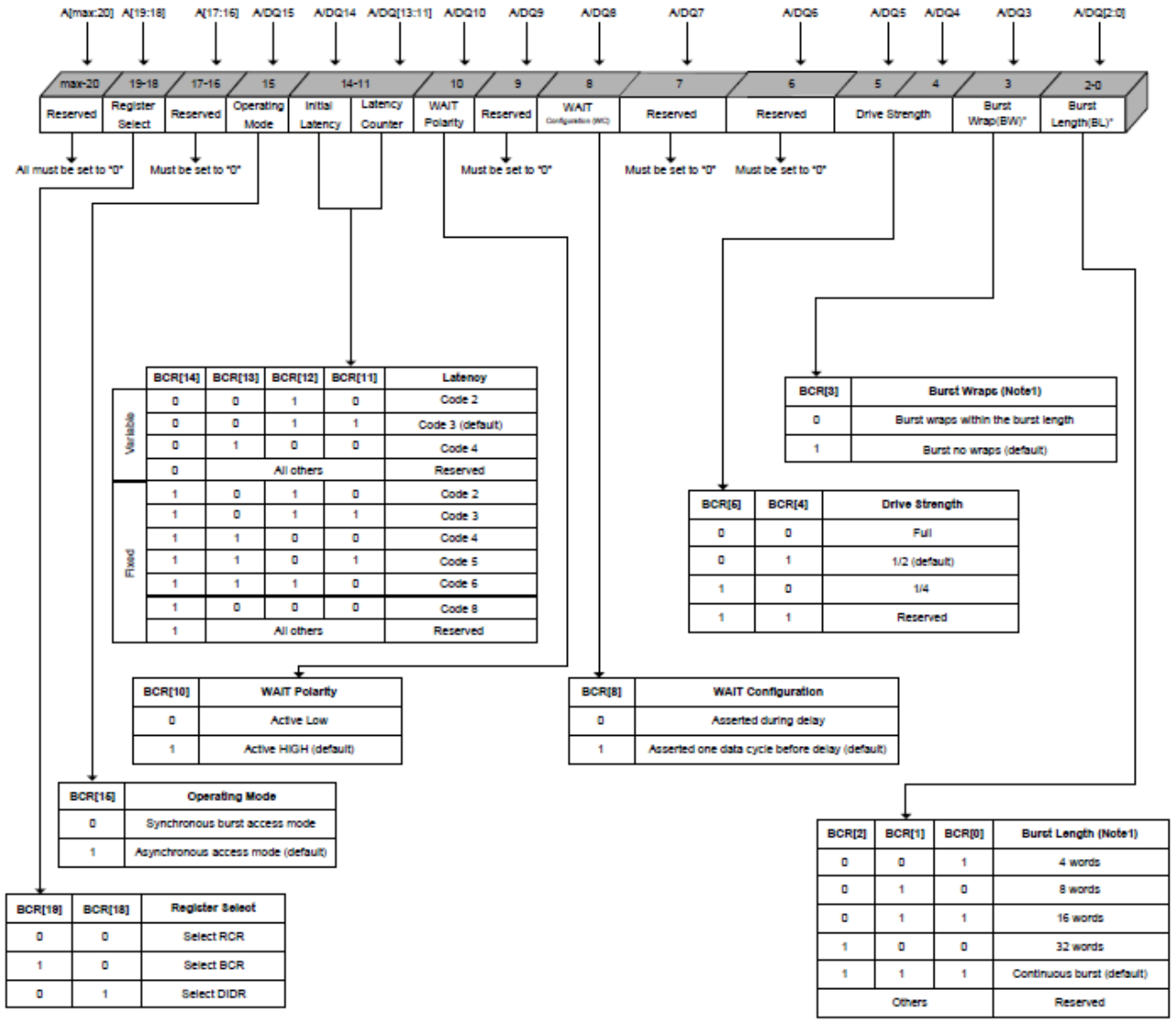
Figure 14: Read Configuration Register



BUS CONFIGURATION REGISTER

The BCR defines how the Cellular RAM device interacts with the system memory bus. Figure 15 describes the control bits in the BCR. At power-up, the BCR is set to 9D1Fh. The BCR is accessed with CRE HIGH and A [19:18] = 10b, or through the register access software sequence with A/DQ = 0001h on the third cycle.

Figure 15: Bus Configuration Register Definition



Notes:

1. Burst wrap and length apply to both READ and WRITE operations.
2. Reserved bits must be set to zero. Reserved bits not set to zero will affect device functionality.
3. BCR [15:0] will be read back as written.

Burst Length (BCR [2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address.

Burst Wrap (BCR [3]) Default = No Wrap

The burst-wrap option determines if a 4, 8, 16, or 32 word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses without regard to address boundaries; the internal address wrap to 000000h if the device is read past the last address.

Table 3: Sequence and Burst Length

Burst Wrap		Start Addr	4-Word Burst Length	8-Word Burst Length	16-Word Burst Length	32-Word Burst Length	Continuous Burst
BCR[3]	Wrap	Deci-mal	Linear	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-...-29-30-31	0-1-2-3-4-5-6-...
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-...-30-31-0	1-2-3-4-5-6-7-...
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-...-31-0-1	2-3-4-5-6-7-8-...
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-...-0-1-2	3-4-5-6-7-8-9-...
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-...-1-2-3	4-5-6-7-8-9-10-...
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-...-2-3-4	5-6-7-8-9-10-11-...
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-...-3-4-5	6-7-8-9-10-11-12-
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-...-4-5-6	7-8-9-10-11-12-13-...
		...			...	...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-...-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-...-12-13-14	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-0-...-27-28-29	30-31-32-33-34-...
		31				31-0-1-...-28-29-30	31-32-33-34-35-...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2...–29-30-31	0-1-2-3-4-5-6-...
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-...-30-31-32	1-2-3-4-5-6-7-...
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-...-31-32-33	2-3-4-5-6-7-8-...
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-...-32-33-34	3-4-5-6-7-8-9-...
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-...-33-34-35	4-5-6-7-8-9-10-...
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20	5-6-7-...-34-35-36	5-6-7-8-9-10-11...
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21	6-7-8-...-35-36-37	6-7-8-9-10-11-12...
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-...-17-18-19-20-21-22	7-8-9-...-36-37-38	7-8-9-10-11-12-13...
		...			...	...	...
		14			14-15-16-17-18-19-...-23-24-25-26-27-28-29	14-15-16-...-43-44-45	14-15-16-17-18-19-20-...
		15			15-16-17-18-19-20-...-24-25-26-27-28-29-30	15-16-17-...-44-45-46	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-32-...-59-60-61	30-31-32-33-34-35-36-...
		31				31-32-33-...-60-61-62	31-32-33-34-35-36-37-...

Drive Strength (BCR [5:4]) Default = Outputs Use Half-Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + Cellular RAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during READ operations. Full output drive strength should be selected when using a discrete Cellular RAM device in a more heavily loaded data bus environment. Outputs are configured at half- drive strength during testing. See Table 4 for additional information.

Table 4: Drive Strength

BCR [5]	BCR [4]	Drive	Impedance Typ	Use Recommendation
0	0	Full	25~30	CL = 30pF to 50pF
0	1	1/2 (default)	50	CL = 15pF to 30pF 108 MHz at light load
1	0	1/4	100	CL = 15pF or lower
1	1	Reserved		

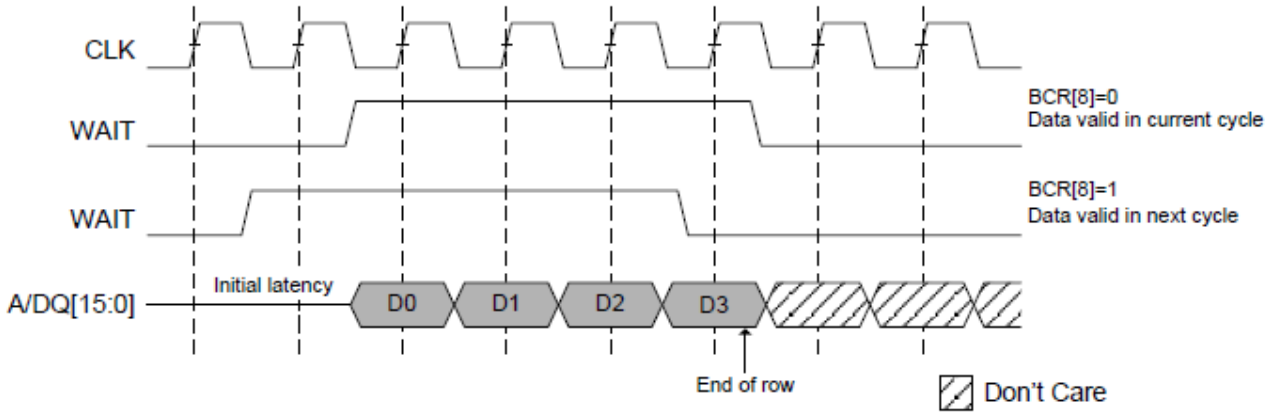
WAIT Configuration (BCR [8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR [8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively. When BCR [8] = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (See Figure 16).

WAIT Polarity (BCR [10]) Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

Figure 16: WAIT Configuration During Burst Operation



Note: Signals shown are for WAIT active LOW, no wrap.

Latency Counter (BCR [13:11]) Default = Three Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes, see Table 5 and 6 on pages 26 and 27, respectively, and Figure 17 and 18 in page 27, respectively.

Initial Access Latency (BCR [14]) Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations. Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter (See Table 6 on page 27 and Figure 18 on page 27).

Table 5: Variable Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency [1]		Max Input CLK Frequency (MHz)			
		Normal	Refresh Collision	133	108	83	48
010	2 (3 clocks)	2	4	66(15ns)	66(15ns)	52(19.2ns)	48(20.8ns)
011	3 (4 clocks)-default	3	6	108(9.26ns)	108(9.26ns)	83(12ns)	-
100	4 (5 clocks)	4	8	133(7.5ns)	-	-	-
Others	Reserved	-	-	-	-	-	-

Figure 17: Latency Counter (Variable Initial Latency, No Refresh Collision)

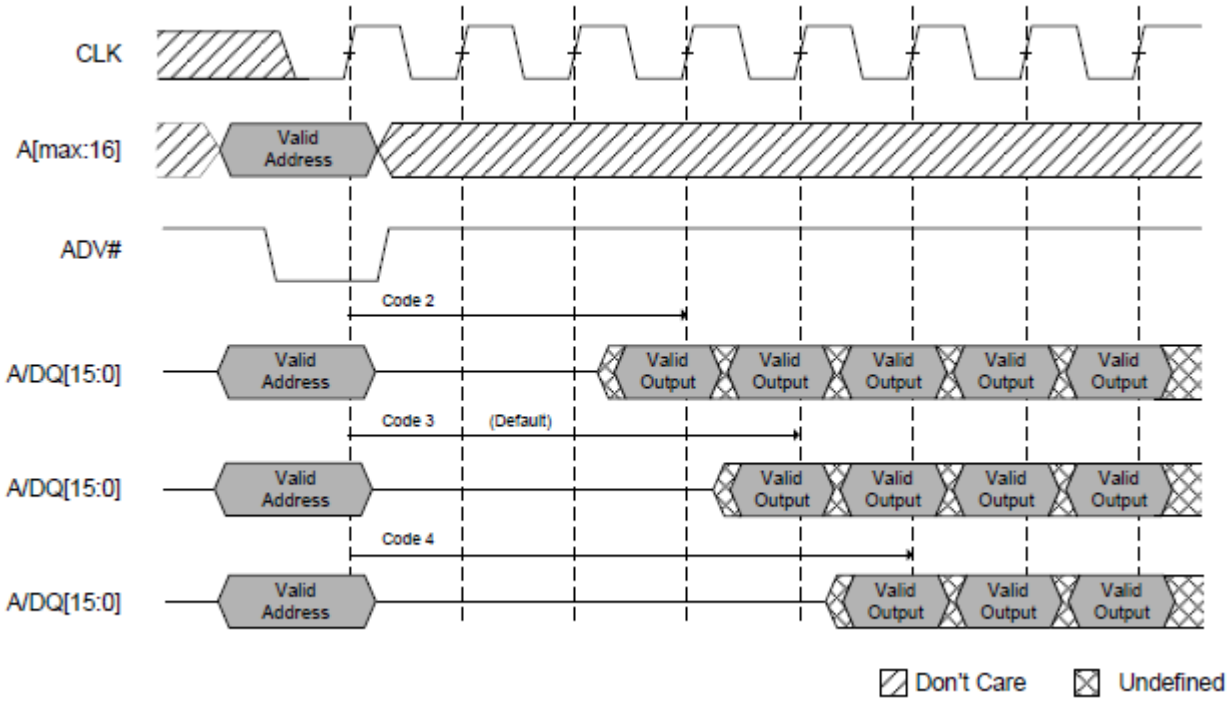
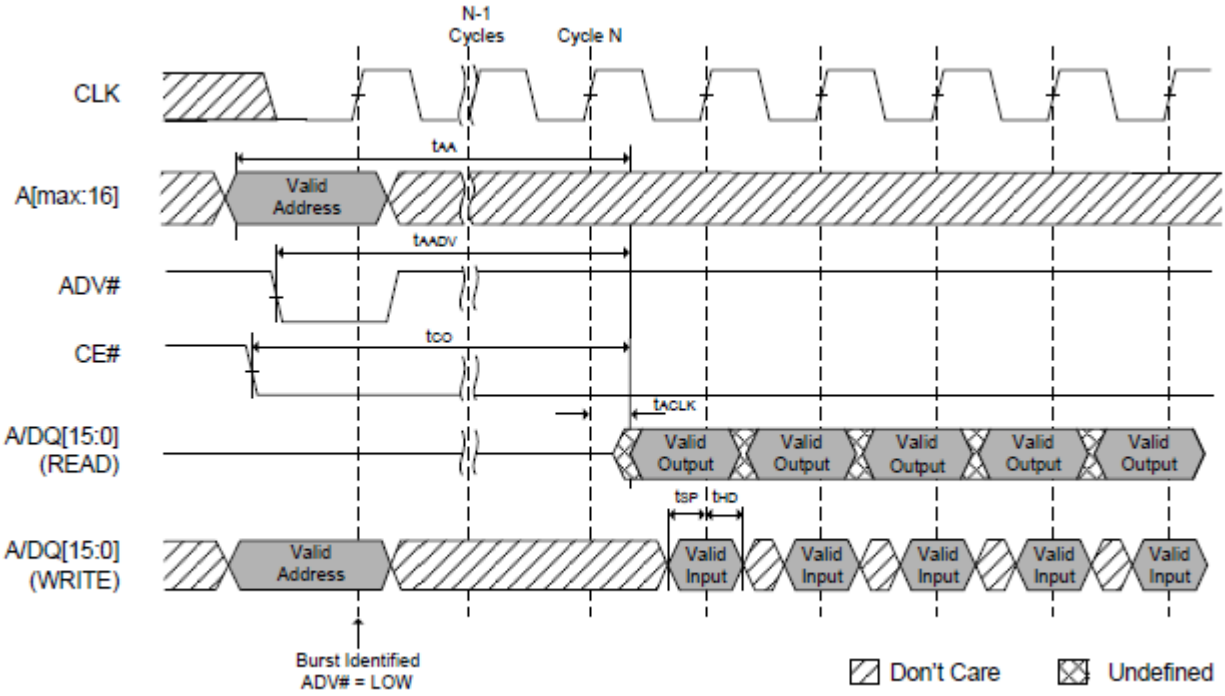


Table 6: Fixed Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency Count (N)	Max Input CLK Frequency (MHz)			
		Normal	133	108	83	48
010	2 (3 clocks)	2	33(30ns)	33(30ns)	33(30ns)	33(30ns)
011	3 (4 clocks)-default	3	52(19.2ns)	52(19.2ns)	52(19.2ns)	48(20.8ns)
100	4 (5 clocks)	4	66(15ns)	66(15ns)	66(15ns)	-
101	5 (6 clocks)	5	75(13.3ns)	75(13.3ns)	75(13.3ns)	-
110	6 (7 clocks)	6	108(9.26ns)	108(9.26ns)	83(12ns)	-
000	8 (9 clocks)	8	133(7.5ns)	-	-	-
Others	Reserved	--	-	-	-	-

Figure 18: Latency Counter (Fixed Latency)



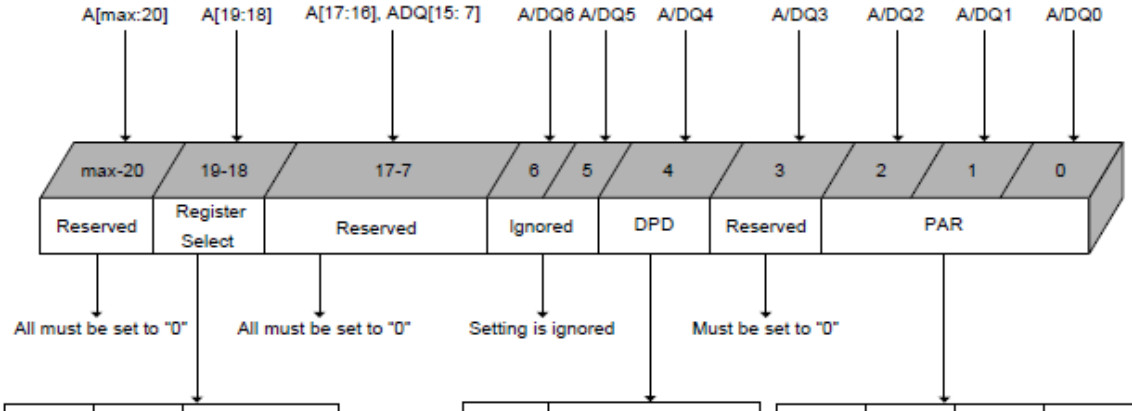
Operating Mode (BCR [15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

REFRESH CONFIGURATION REGISTER

The refresh configuration register (RCR) defines how the Cellular RAM device performs its transparent self-refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Figure 19 describes the control bits used in the RCR. At power-up, the RCR is set to 0010h. The RCR is accessed with CRE HIGH and A [19:18] = 00b; or through the register access software sequence with A/DQ = 0000h on the third cycle.

Figure 19: Refresh Configuration Register Mapping



RCR[19]	RCR[18]	Register Select
0	0	Selsect RCR
1	0	Selsect BCR
0	1	Selsect DIDR

RCR[4]	Deep Power-Down
0	DPD Enable
1	DPD Disable (default)

RCR[2]	RCR[1]	RCR[0]	Refersh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

Note:

Reserved bits must be set to zero. Reserved bits not set to zero will affect device functionality. RCR [15:0] will be read back as written.

Partial Array Refresh (RCR [2:0] Default = Full Array Refresh)

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (See Table 7 and Table 8).

Table 7: Address Patterns for PAR (RCR [4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full Die	000000h-3FFFFFh	4 Meg x 16	64Mb
0	0	1	One-half die	000000h-1FFFFFh	2 Meg x 16	32Mb
0	1	0	One-quarter of die	000000h-0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h-07FFFFh	512 K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	200000h-3FFFFFh	2 Meg x 16	32Mb
1	1	0	One-quarter of die	300000h-3FFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	380000h-3FFFFFh	512 K x 16	8Mb

Deep Power-Down (RCR [4]) Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the Cellular RAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re- enabled, the Cellular RAM device will require 150µs to perform an initialization procedure before normal operations can resume. Deep power-down is enabled by setting RCR [4] = 0 and taking CE# HIGH. DPD can be enabled using CRE or the software sequence to access the RCR. Taking CE# LOW for at least 10µs disables DPD and sets RCR [4] = 1; it is not necessary to write to the RCR to disable DPD. BCR and RCR values (other than RCR [4]) are preserved during DPD.

Device Identification Register

The DIDR provides information on the device manufacturer, Cellular RAM generation, and the specific device configuration. This register is read-only. The DIDR is accessed with CRE HIGH and A [19:18] = 01b, or through the register access software sequence with A/DQ = 0002h on the third cycle.

ELECTRICAL CHARACTERISTICS

Table 8: Absolute Maximum Ratings

Parameter	Rating
Voltage to any pin except Vcc, VccQ relative to Vss	-0.3V to VccQ + 0.3V
Voltage on Vcc supply relative to Vss	-0.2V to +2.45V
Voltage on VccQ supply relative to Vss	-0.2V to +2.45V
Storage temperature (plastic)	-55°C to +150°C
Operating temperature (case) Wireless	-30°C to +85°C
Operating temperature (case) Industrial	-40°C to +85°C
Soldering temperature and time: 10s (solder ball only) +260°C	

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9: Electrical Characteristics and Operating Conditions

Wireless Temperature (-30°C < T_C < +85°C), Industrial Temperature (-40°C < T_C < +85°C)

Description	Conditions	Symbol		Min	Max	Unit	Notes
Supply voltage		V_{CC}		1.7	1.95	V	
I/O supply voltage		V_{CCQ}		1.7	1.95	V	
Input high voltage		V_{IH}		V_{CCQ} - 0.4	V_{CCQ} + 0.2	V	1
Input low voltage		V_{IL}		-0.20	0.4	V	2
Output high voltage	I_{OH} = -0.2mA	V_{OH}		0.80 V_{CCQ}		V	3
Output low voltage	I_{OL} = +0.2mA	V_{OL}			0.20 V_{CCQ}	V	3
Input leakage current	V_{IN} = 0 to V_{CCQ}	I_{LI}			1	µA	
Output leakage current	OE# = V_{IH} or chip disabled	I_{LO}			1	µA	
Operating current	**Conditions**	**Symbol**		**Typ**	**Max**	**Unit**	**Notes**
Asynchronous random READ/WRITE	V_{IN} = V_{CCQ} or 0V chip enabled, I_{OUT} = 0	$I_{CC}1$	70ns		25	mA	4
Initial access, burst READ/WRITE		$I_{CC}2$	133MHz		40	mA	4
			108MHz		35	mA	
			83MHz		30	mA	
			48MHz		20	mA	
Continuous burst READ		$I_{CC}3R$	133MHz		35	mA	4
			108MHz		30	mA	
			83MHz		25	mA	
			48MHz		20	mA	
Continuous burst WRITE		$I_{CC}3W$	133MHz		40	mA	4
			108MHz		35	mA	
			83MHz		30	mA	
			48MHz		20	mA	
Standby current	V_{IN} = V_{CCQ} or 0V, CE# = V_{CCQ}	I_{SB}	Standard	50	90	µA	5, 6

Note:

1. Input signals may overshoot to VCCQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to VSS - 1.0V for periods less than 2ns during transitions.
3. BCR [5:4] = 01b (default setting of one-half drive strength).
4. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
5. ISB (max) values measured with PAR set to FULL ARRAY and at +85°C. In order to achieve low standby current, all inputs must be driven to either VCCQ or VSS. ISB might be slightly higher for up to 500ms after power-up, or when entering standby mode.
6. ISB (typ) is the average ISB at 25°C and VCC = VCCQ = 1.8V. This parameter is verified during characterization and is not 100% tested.

Table 10: Deep Power-Down Specifications

Description	Conditions	Symbol	Typ	Max	Unit
Deep Power-Down	V_{IN} = VccQ or 0V; Vcc, VccQ = 1.95V; +85°C	I_{ZZ}	5	20	μA

Note: Typical (TYP) I_{ZZ} value is tested at Vcc=1.8V, T_A=25°C .This parameter is verified during characterization and is not 100% tested.

Table 11: Partial-Array Refresh Specifications and Conditions

Description	Conditions	Symbol		Array	Max	Unit
Partial array refreshes standby current	V_{IN} = V_{CCQ} or 0V, CE# = V_{CCQ}	I_{PAR}	Standard power (no designation)	Full	90	uA
				1/2	65	
				1/4	55	
				1/8	50	
				0	45	

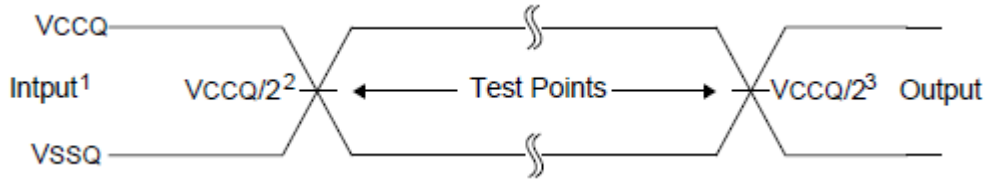
Note: IPAR (MAX) values measured at 85°C. IPAR might be slightly higher for up to 500 ms after changes to the PAR array partition or when entering standby mode.

Table 12: Capacitance

Description	Conditions	Symbol	Min	Max	Unit	Notes
Input Capacitance	Tc = = +25°C; f = 1 MHz; V_{IN} = 0V	C_{IN}	2.0	6	pF	1
Input/output Capacitance		C_{IO}	3.0	6.5	pF	1

Note: 1. These parameters are verified in device characterization and are not 100% tested.

Figure 20: AC Input/output Reference Waveform



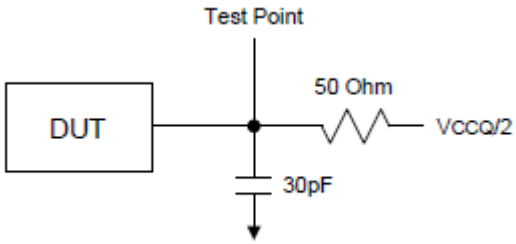
Notes:

1. AC test inputs are driven at VCCQ for a logic 1 and VSSQ for a logic 0. Input rise and fall times (10% to 90%) <1.6ns.

2. Input timing begins at VCCQ/2.

3. Output timing ends at VCCQ/2.

Figure 21: AC Output Load Circuit



Note: All tests are performed with the outputs configured for default setting of half drive strength (BCR [5:4] = 01b).

TIMING REQUIREMENTS

Table 13: Asynchronous READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR [5:4] = 01b).

Parameter	Symbol	Min	Max	Unit	Notes
Address access time	t_{AA}		70	ns	
ADV# access time	t_{AADV}		70	ns	
Address hold from ADV# HIGH	t_{AVH}	2		ns	
Address setup to ADV# HIGH	t_{AVS}	5		ns	
LB#/UB# access time	t_{BA}		70	ns	
LB#/UB# disable to DQ High-Z	t_{BHZ}		7	ns	1
Chip select access time	t_{CO}		70	ns	
CE# LOW to ADV# HIGH	t_{CVS}	7		ns	
Chip disable to DQ and WAIT High-Z	t_{HZ}		7	ns	1
Output enable to valid output	t_{OE}		20	ns	
OE# LOW to WAIT valid	t_{OEW}	1	7.5	ns	
Output disable to DQ High-Z output	t_{OHZ}		7	ns	1
Output enable to Low-Z output	t_{OLZ}	3		ns	2
ADV# pulse width	t_{VP}	5		ns	

Note:

1. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.
2. The Low-Z timings measure a 100mV transition away from the High-Z (VccQ/2) level toward either V_{OH} or V_{OL}.

3.

Table 14: Burst READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR [5:4] = 01b).

Parameter	Symbol	133MHz		108MHz		83MHZ		48MHZ		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Address access time (fixed latency)	t_{AA}		70		70		70		0	ns	
ADV# access time (fixed latency)	t_{AADV}		70		70		70		70	ns	
Burst to READ access time (variable latency)	t_{ABA}		35.5		35.9		45		50.6	ns	
CLK to output delay	t_{ACLK}		5.5		7		9		9	ns	
Address hold from ADV# HIGH (fixed latency)	t_{AVH}	2		2		2		2		ns	
Burst OE# LOW to output delay	t_{BOE}		20		20		20		20	ns	
CE# HIGH between subsequent burst or mixed mode operations	t_{CBPH}	5		5		6		6		ns	1
Maximum CE# pulse width	t_{CEM}		4		4		4		4	ns	1
CLK period	t_{CLK}	7.5		9.26		12		20.8		ns	
Chip select access time (fixed latency)	t_{CO}		70		70		70		70	ns	
CE# setup time to active CLK edge	t_{CSP}	2.5		3		4		4		ns	
Hold time from active CLK edge	t_{HD}	1.5		2		2		2		ns	
Chip disable to DQ and WAIT High-Z output	t_{HZ}		7		7		7		7	ns	2
CLK rise or fall time	t_{KHKL}		1.2		1.6		1.8		1.8	ns	
CLK to WAIT valid	t_{KHTL}		5.5		7		9		9	ns	
Output HOLD from CLK	t_{KOH}	2		2		2		2		ns	
CLK HIGH or LOW time	t_{KP}	3		3		4		4		ns	
Output disable to DQ High-Z output	t_{OHZ}		7		7		7		7	ns	2
Output enable to Low-Z output	t_{OLZ}	3		3		3		3		ns	3
Setup time to active CLK edge	t_{SP}	2		3		3		3		ns	

Note:

1. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.
3. The Low-Z timings measure a 100mV transition away from the High-Z (VccQ/2) level toward either V_{OH} or V_{OL}.

Table 15: Asynchronous WRITE Cycle Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes
Address and ADV# LOW setup time to WE# LOW	t_{AS}	0		ns	
Address HOLD from ADV# going HIGH	t_{AVH}	2		ns	
Address setup to ADV# going HIGH	t_{AVS}	5		ns	
Address valid to end of WRITE	t_{AW}	70		ns	
LB#/UB# select to end of WRITE	t_{BW}	70		ns	
CE# HIGH between subsequent async operations	t_{CPH}	5		ns	
CE# LOW to ADV# HIGH	t_{CVS}	7		ns	
Chip enable to end of WRITE	t_{CW}	70		ns	
Data HOLD from WRITE time	t_{DH}	0		ns	
Data WRITE setup time	t_{DW}	20		ns	
Chip disable to WAIT High-Z output	t_{HZ}		7	ns	1
ADV# pulse width	t_{VP}	5		ns	
ADV# setup to end of WRITE	t_{VS}	70		ns	
Write to DQ High-Z output	t_{WHZ}		7	ns	1
WRITE pulse width	t_{WP}	45		ns	2

Note:

1. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.
2. WE# Low time must be limited to t_{CEM} (4µs).

Table 16: Burst WRITE Cycle Timing Requirements

Parameter	Symbol	133MHz		108MH		83MHZ		48MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Address and ADV# LOW setup time	t_{AS}	0		0		0		0		ns	1
Address HOLD from ADV# HIGH (fixed latency)	t_{AVH}	2		2		2		2		ns	
CE# HIGH between subsequent burst or mixed mode operations	t_{CBPH}	5		5		6		6		ns	2
Maximum CE# pulse width	t_{CEM}		4		4		4		4	ns	2
Clock period	t_{CLK}	7.5		9.26		12		20.8		ns	
CE# setup to CLK active edge	t_{CSP}	2.5		3		4		4		ns	
Hold time from active CLK edge	t_{HD}	1.5		2		2		2		ns	
Chip disable to WAIT High-Z output	t_{HZ}		7		7		7		7	ns	3
CLK rise or fall time	t_{KHKL}		1.2		1.6		1.8		1.8	ns	
Clock to WAIT valid	t_{KHTL}		5.5		7		9		9	ns	
CLK HIGH or LOW time	t_{KP}	3		3		4		4		ns	
Setup time to activate CLK edge	t_{SP}	2		3		3		3		ns	

Note:

1. t_{AS} required if t_{CSP} > 20ns.
2. A refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
3. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward VccQ/2.

TIMING DIAGRAMS

Figure 22: Initialization Period

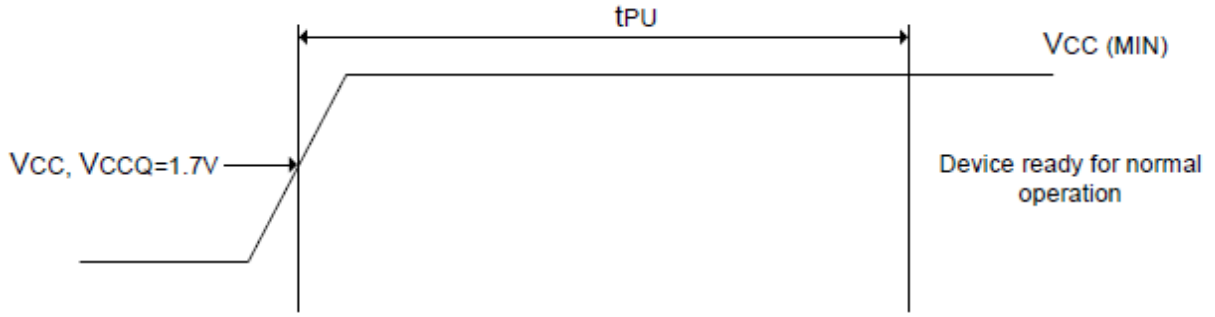


Figure 23: DPD Entry and Exit Timing Parameters

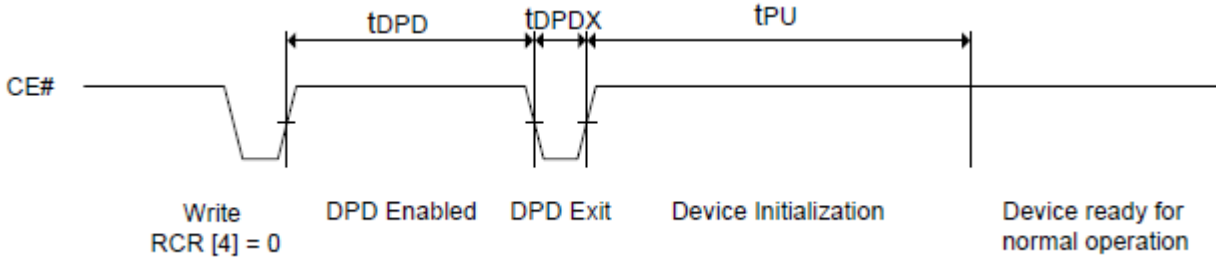


Table 17: Initialization and DPD Timing Parameters

Symbol	Min	Max	Unit
t_{DPD}	150		us
t_{DPDX}	10		us
t_{PU}		150	us

Figure 24: Asynchronous READ

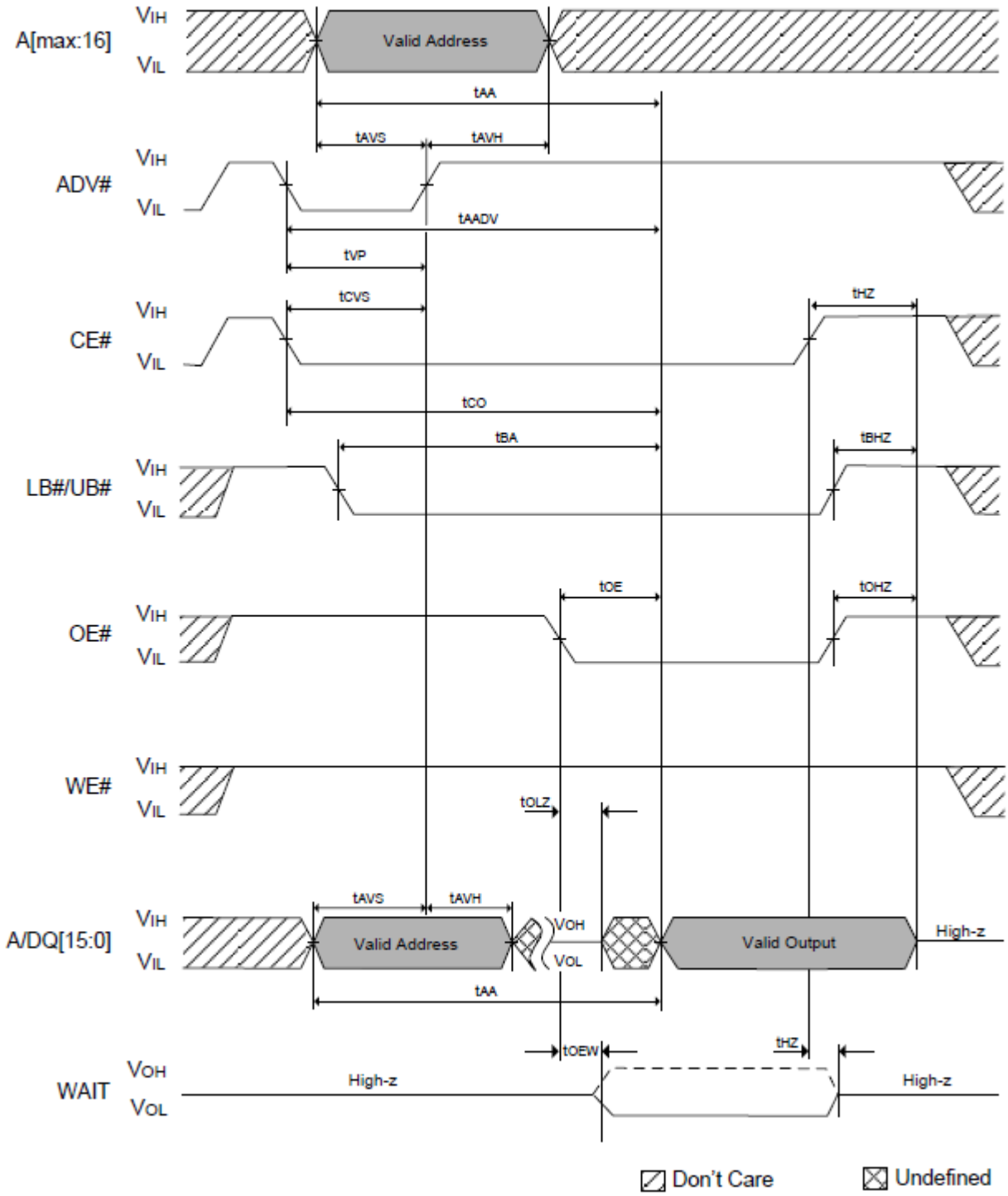
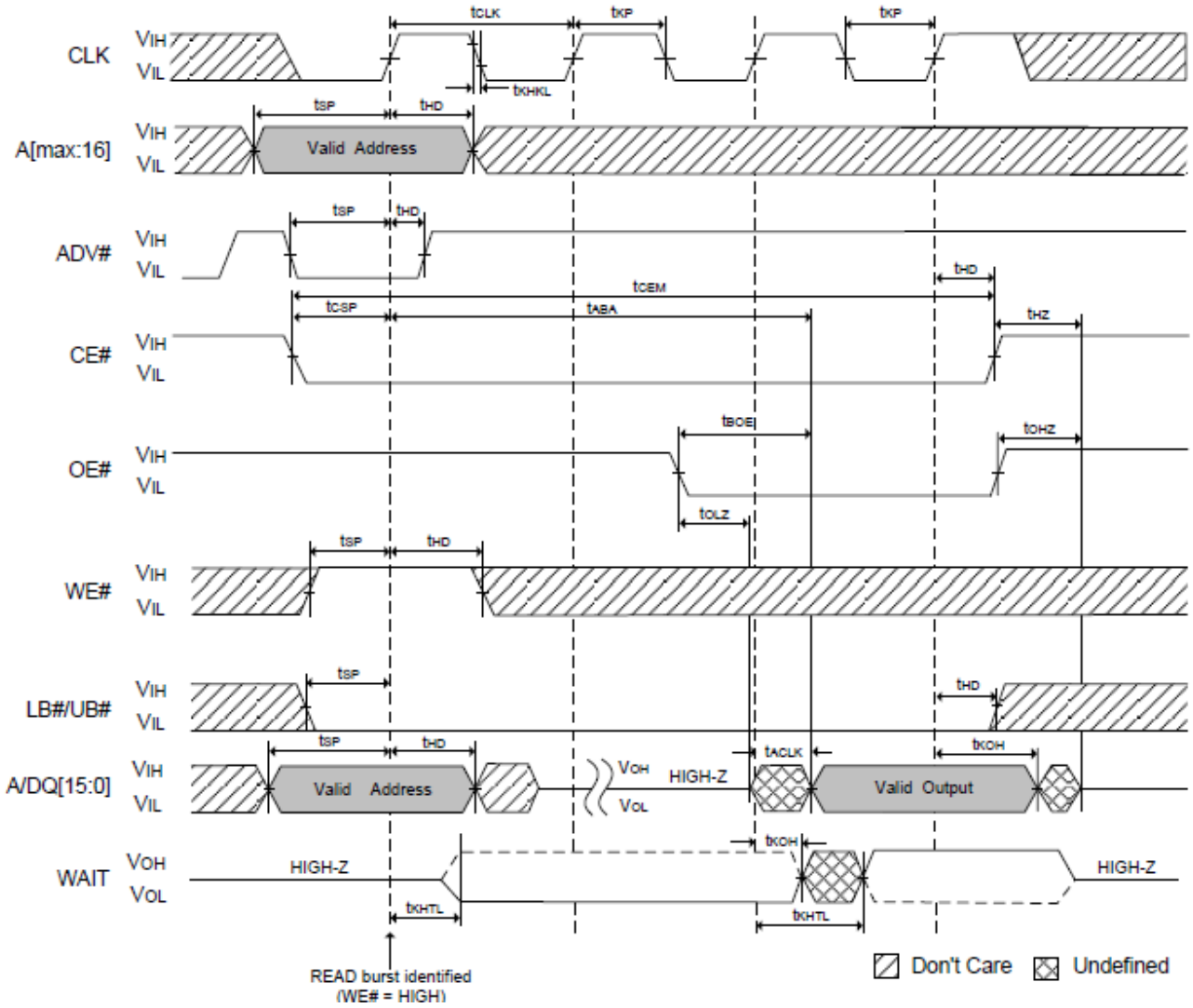
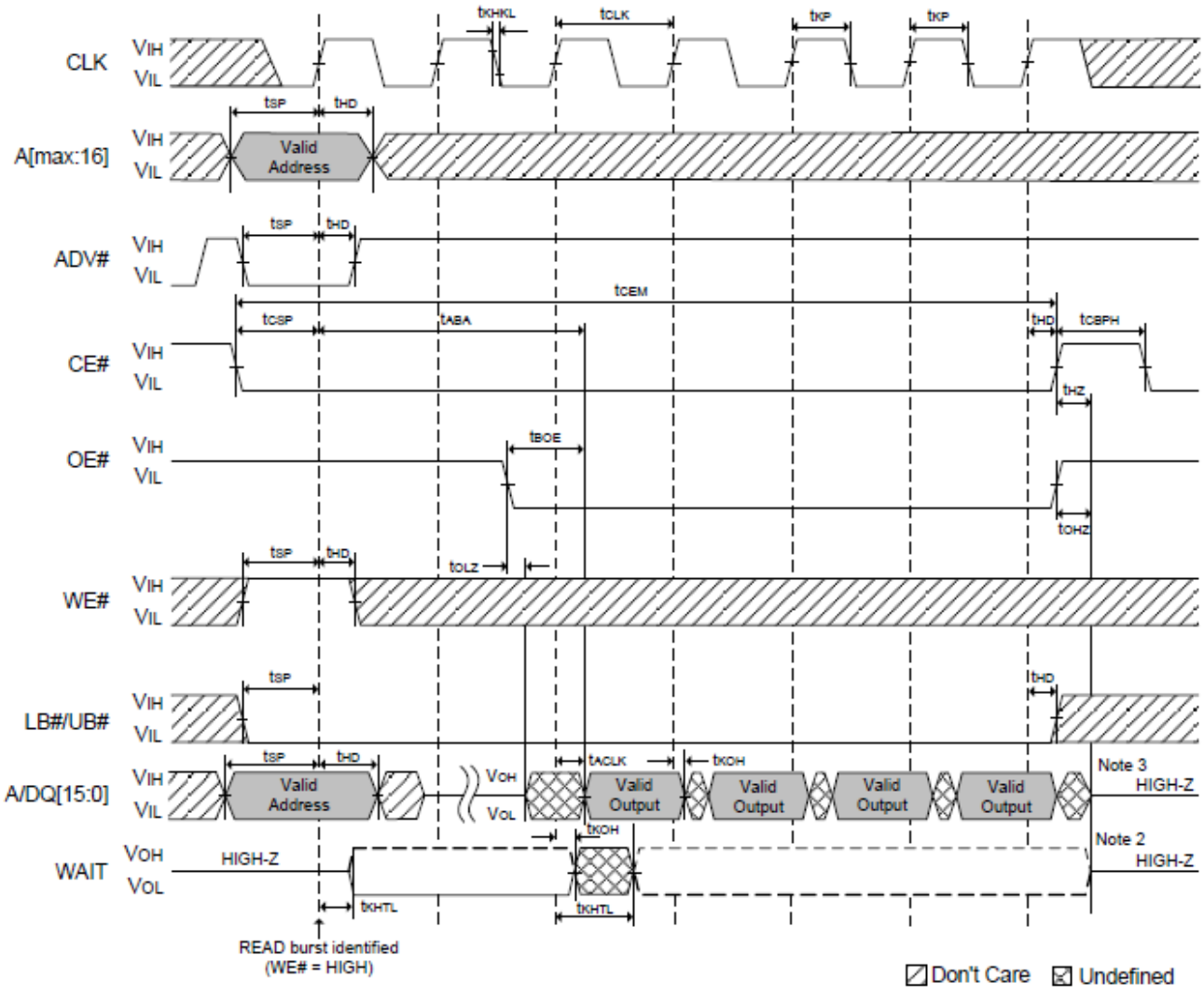


Figure 25: Single-Access Burst READ Operation - Variable Latency



Note: Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

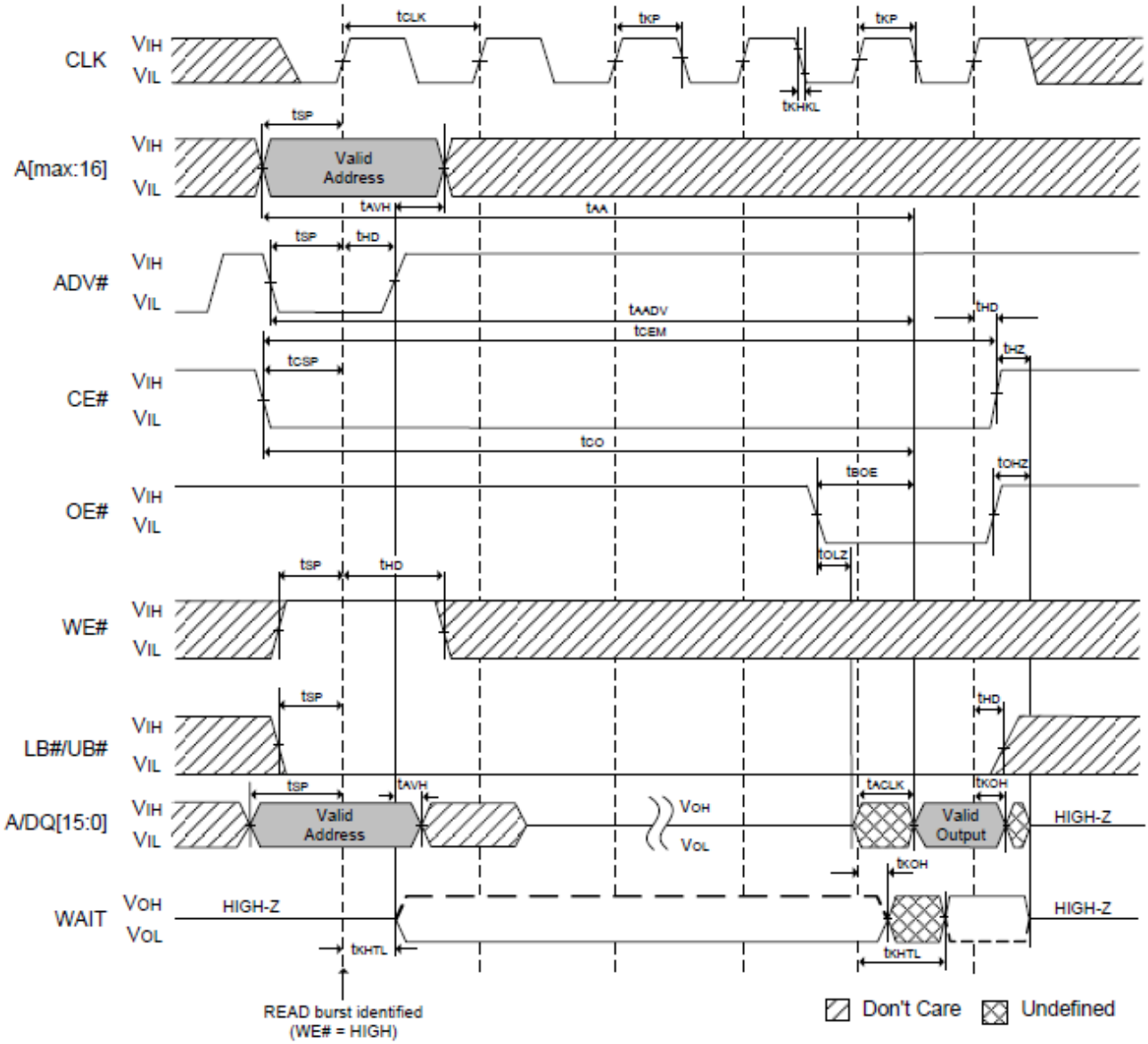
Figure 26: 4-Word Burst READ Operation - Variable Latency



Notes:

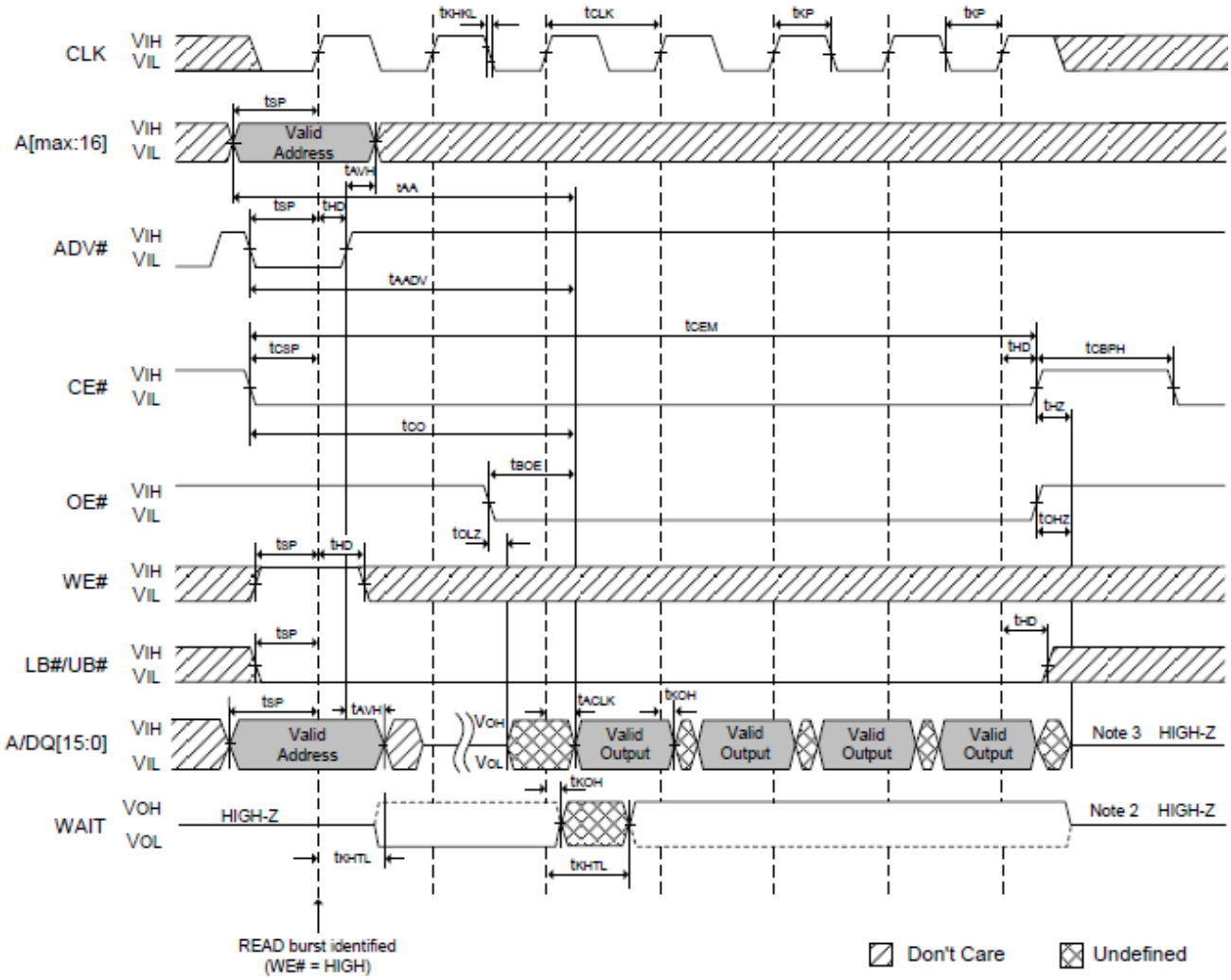
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. WAIT Will remain de-asserted even if CE# remains LOW past the end of the defined burst length.
3. A/DQ [15:0] will output undefined data if CE# remains LOW past the end of the defined burst length.

Figure 27: Single-Access Burst READ Operation - Fixed Latency



Note: Non-default BCR settings: Fixed latency; latency code four (five clocks); WAIT active LOW; WAIT asserted during delay.

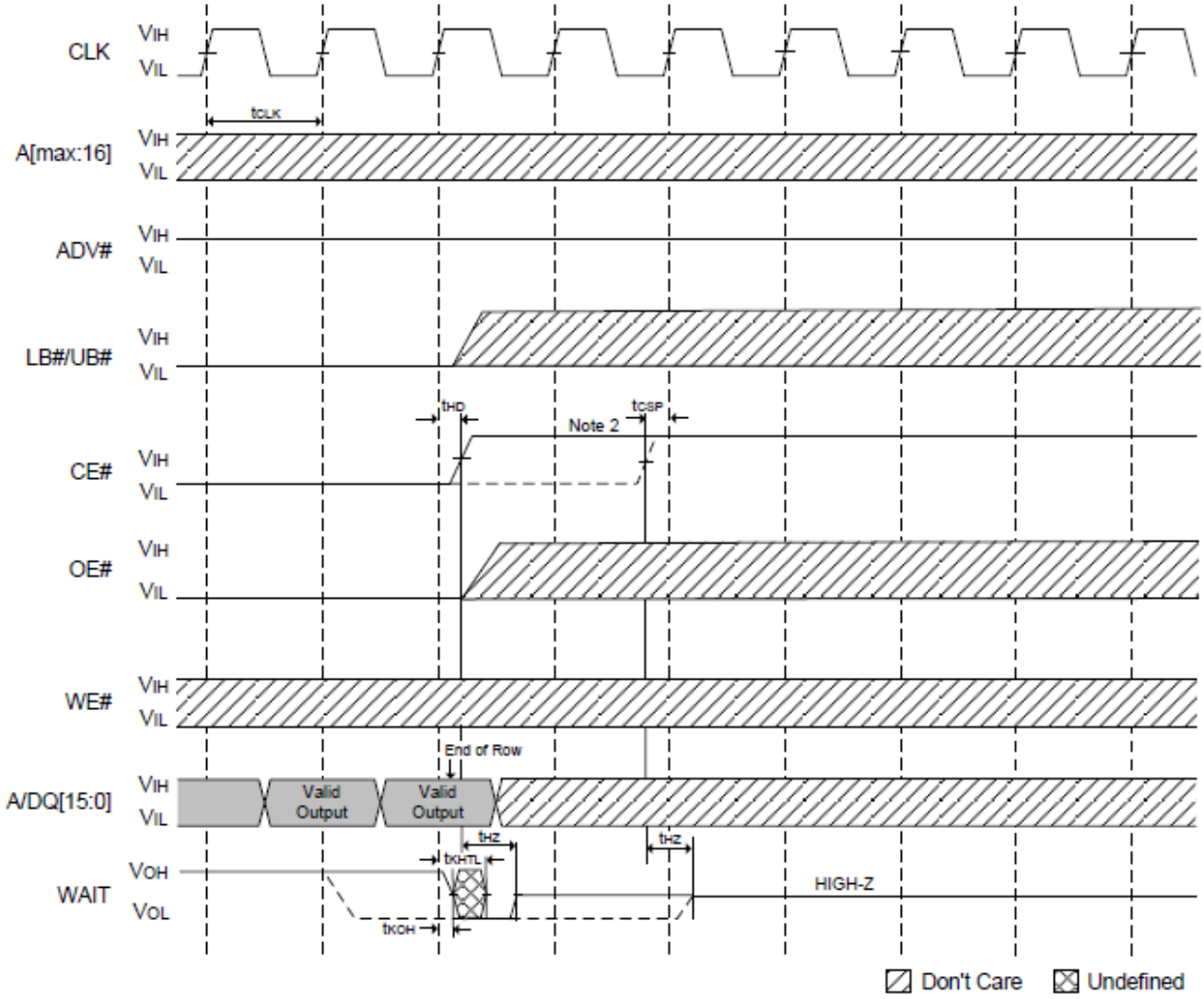
Figure 28: 4-Word Burst READ Operation - Fixed Latency



Notes:

1. Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. WAIT will remain de-asserted even if CE# remains LOW past the end of the defined burst length.
3. A/DQ [15:0] will output undefined data if CE# remains LOW past the end of the defined burst length.

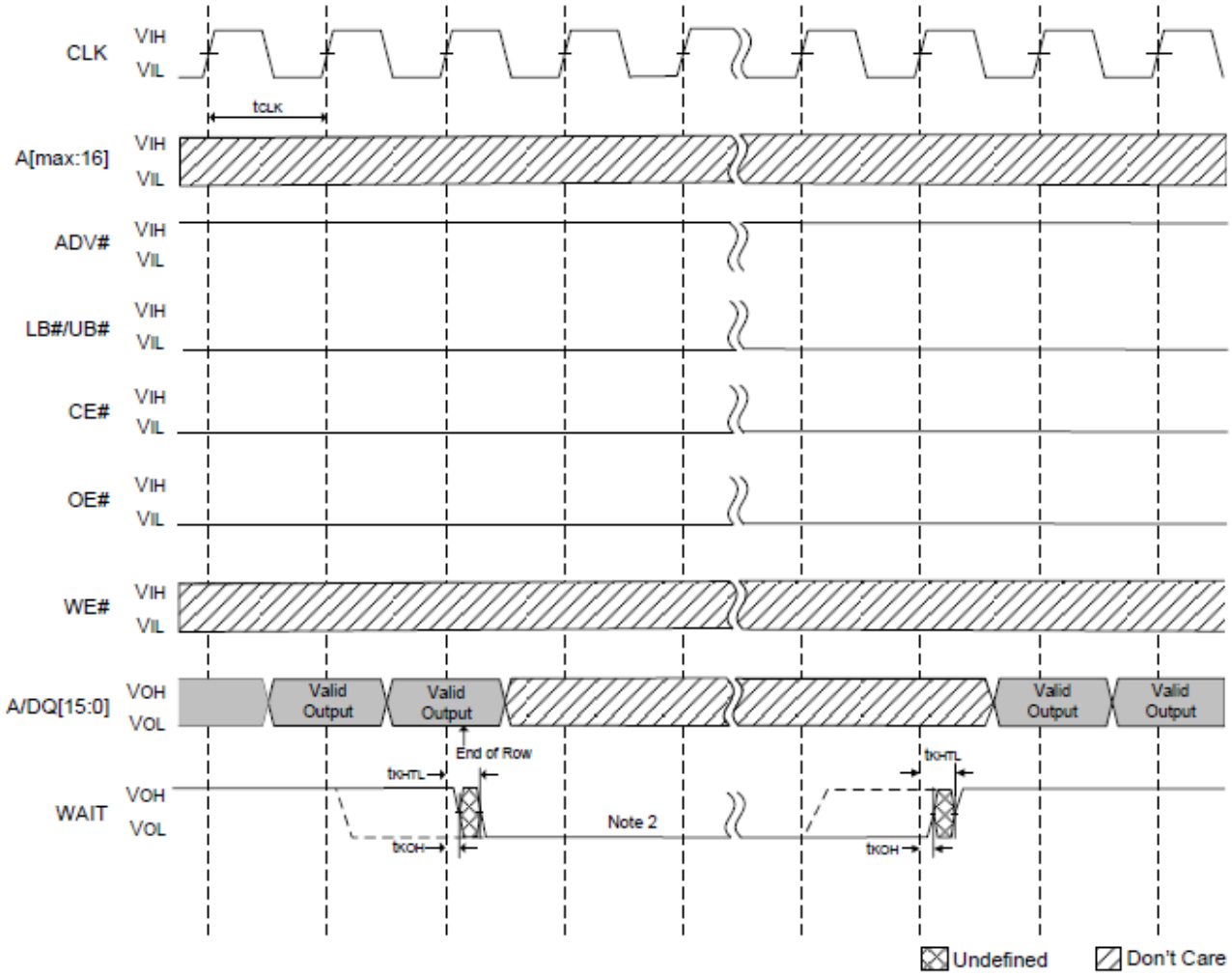
Figure 29: Burst READ Terminate at End-of-Row (Wrap Off)



Notes:

1. Non-default BCR settings for burst READ at end of row: fixed or variable latency, WAIT active LOW, WAIT asserted during delay (shown as solid line).
2. For burst READs, CE# must go HIGH before the second CLK after the WAIT period begins (before the second CLK after WAIT asserts with BCR [8] = 0, or before the third CLK after WAIT asserts with BCR [8] = 1).

Figure 30: Burst READ Row Boundary Crossing



Notes:

1. Non-default BCR settings for burst READ at end of row: fixed or variable latency, WAIT active LOW, WAIT asserted during delay (shown as solid line).
2. WAIT will be asserted LC+1 cycle for variable latency or fixed latency.

Figure 31: Asynchronous WRITE

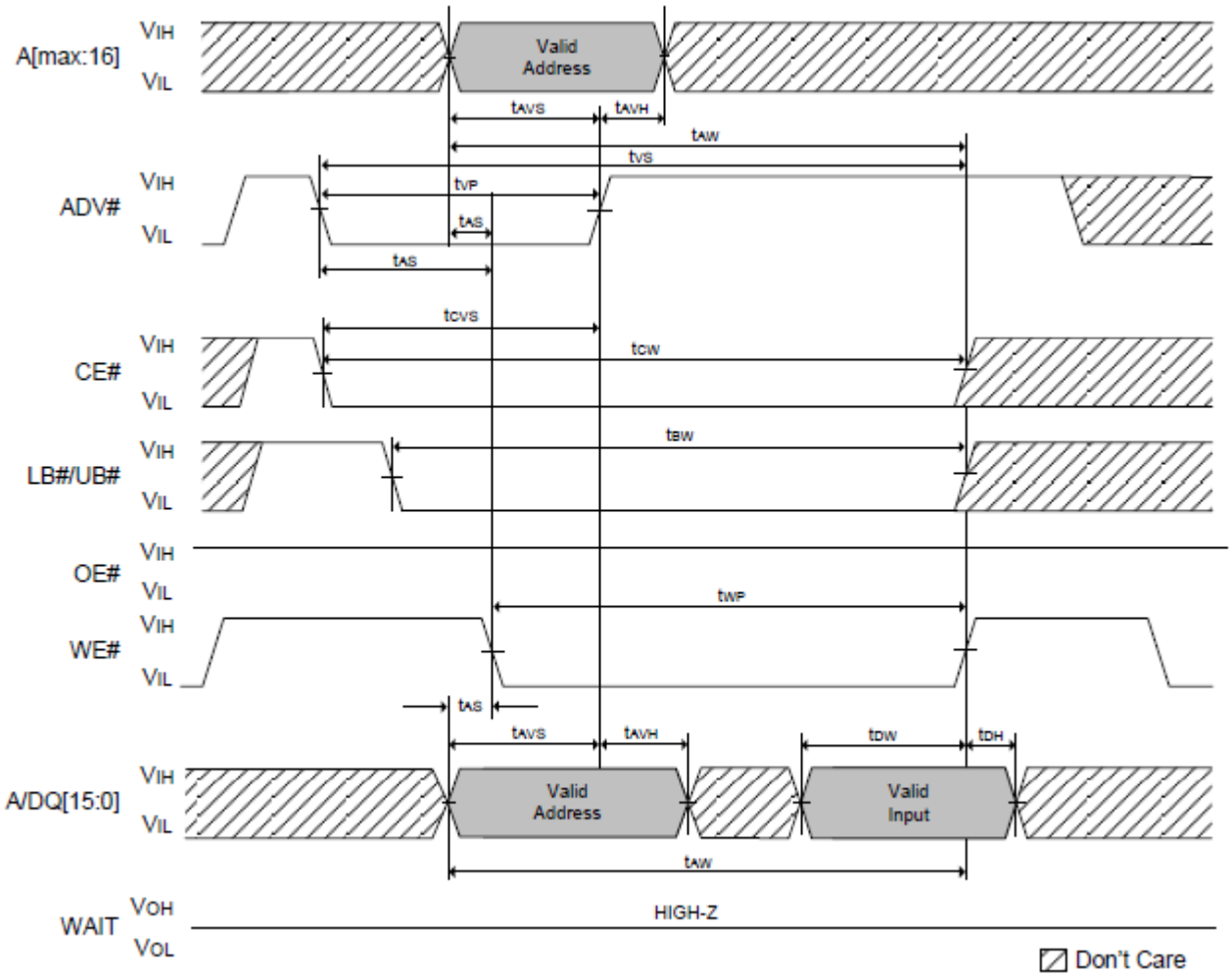
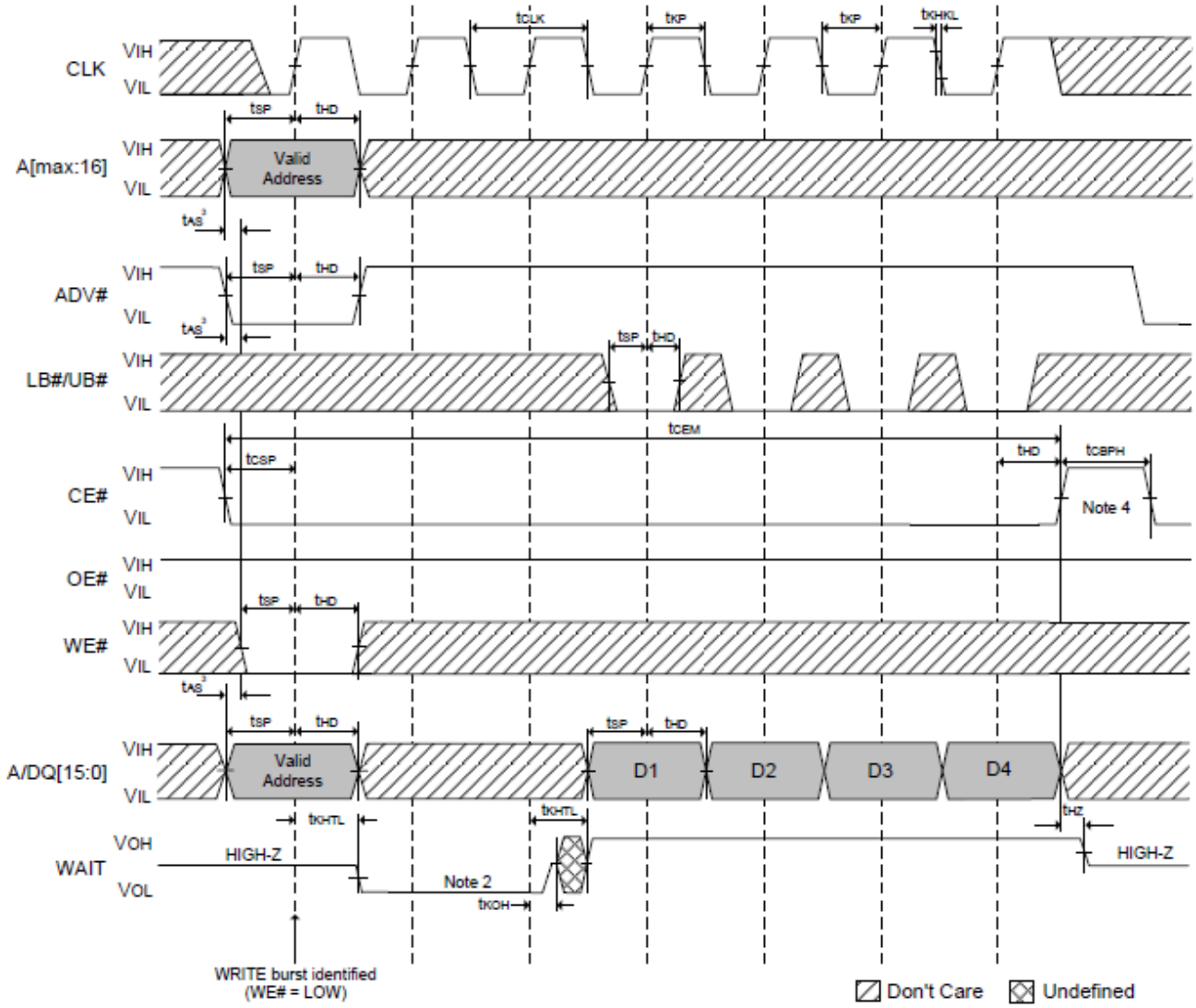


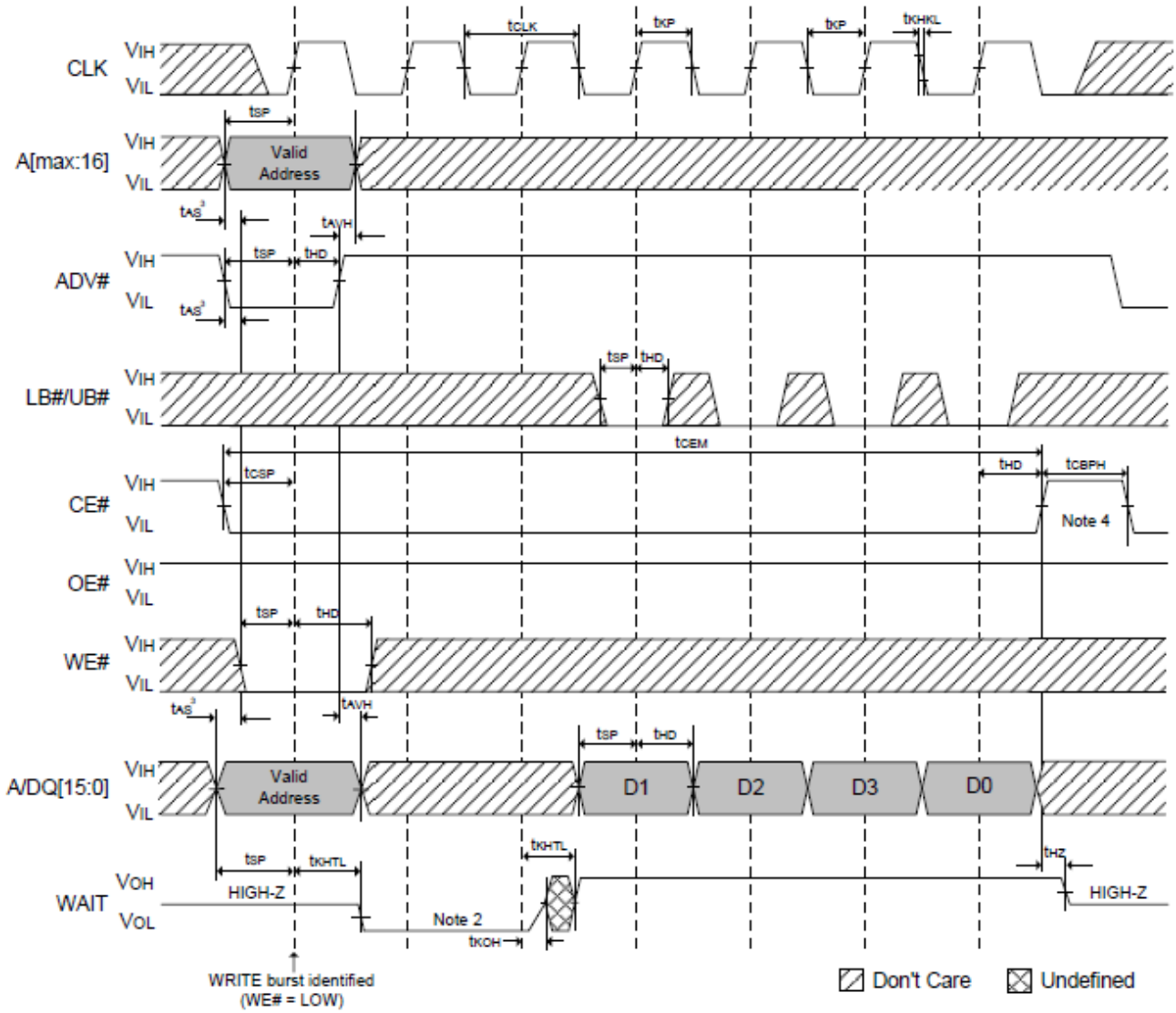
Figure 32: Burst WRITE Operation - Variable Latency Mode



Notes:

1. Non-default BCR settings for burst WRITE operation in variable latency mode: latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay, burst length 4, burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = latency code (BCR [13:11]).
3. tAS is required if tCSP > 20ns.
4. CE# must go HIGH before any clock edge following the last word of a defined-length burst.

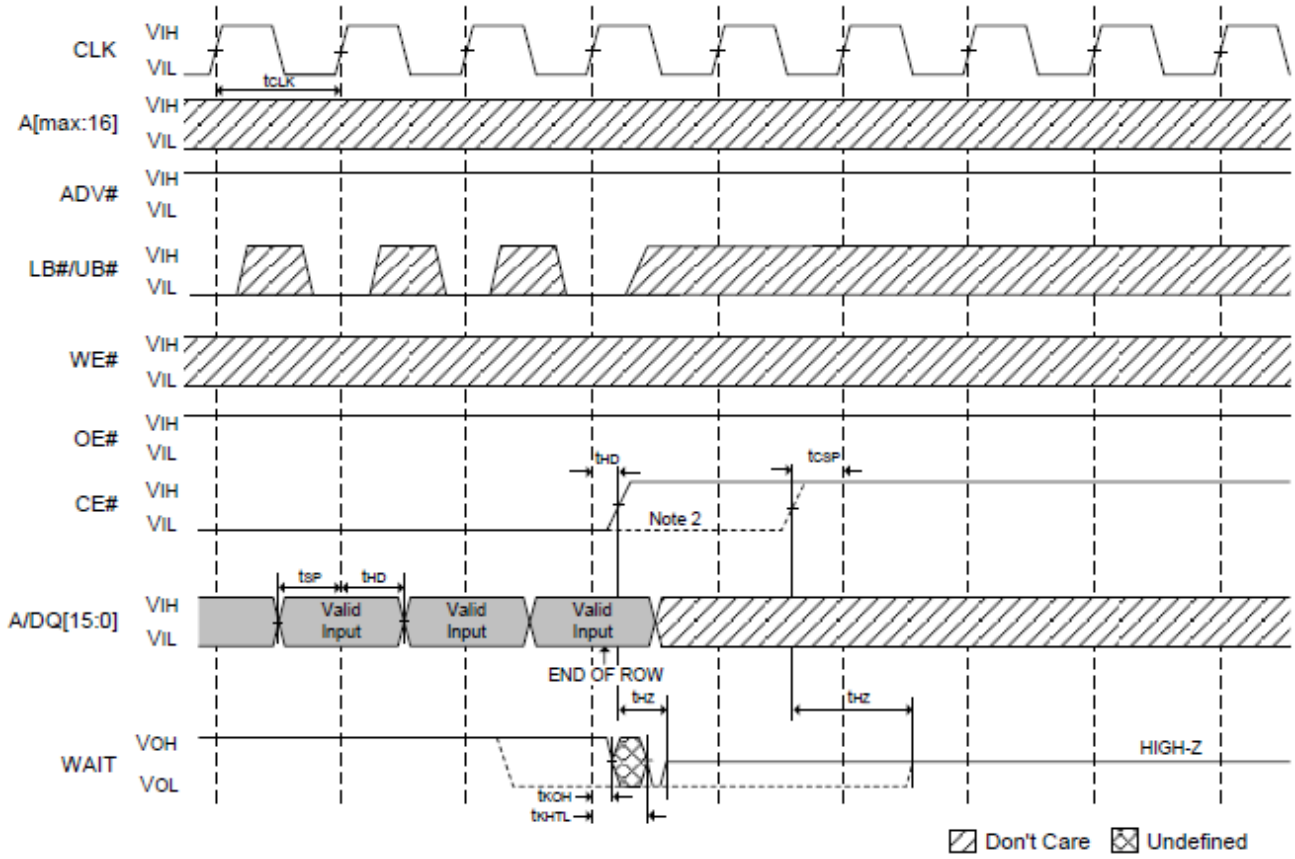
Figure 33: Burst WRITE Operation - Fixed Latency Mode



Notes:

1. Non-default BCR settings for burst WRITE operation in fixed latency mode: fixed latency, latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay, burst length 4, burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = latency code (BCR [13:11]).
3. tAS is required if tCSP > 20ns.
4. CE# must go HIGH before any clock edge following the last word of a defined-length burst.

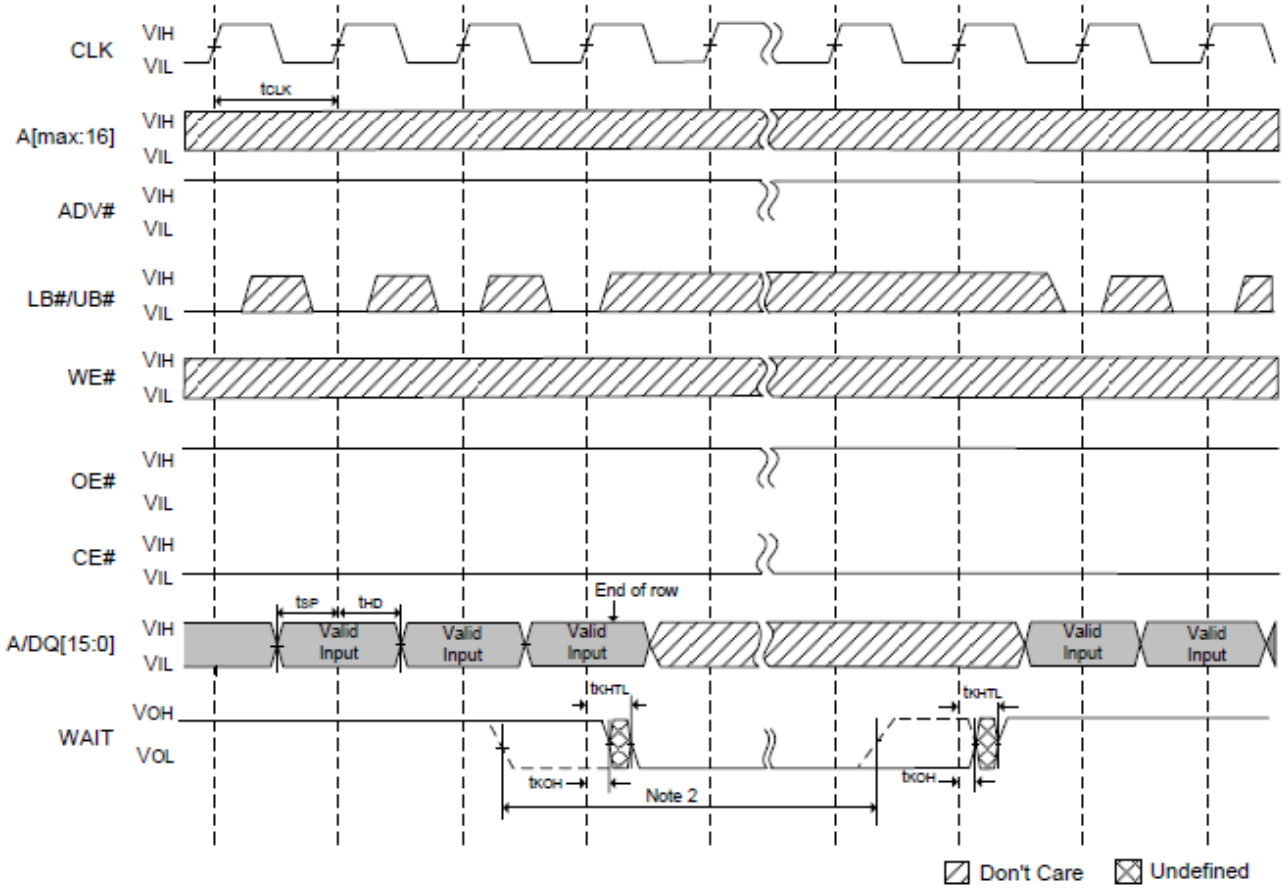
Figure 34: Burst WRITE Terminate at End-of-Row (Wrap Off)



Note:

1. Nondefault BCR settings for burst WRITE at end of row: fixed or variable latency, WAIT active LOW, WAIT asserted during delay. (shown as solid line)
2. For burst WRITEs, CE# must go HIGH before the second CLK after the WAIT period begins (before the second CLK after WAIT asserts with BCR [8] =0, or before the third CLK after WAIT asserts with BCR [8] =1).

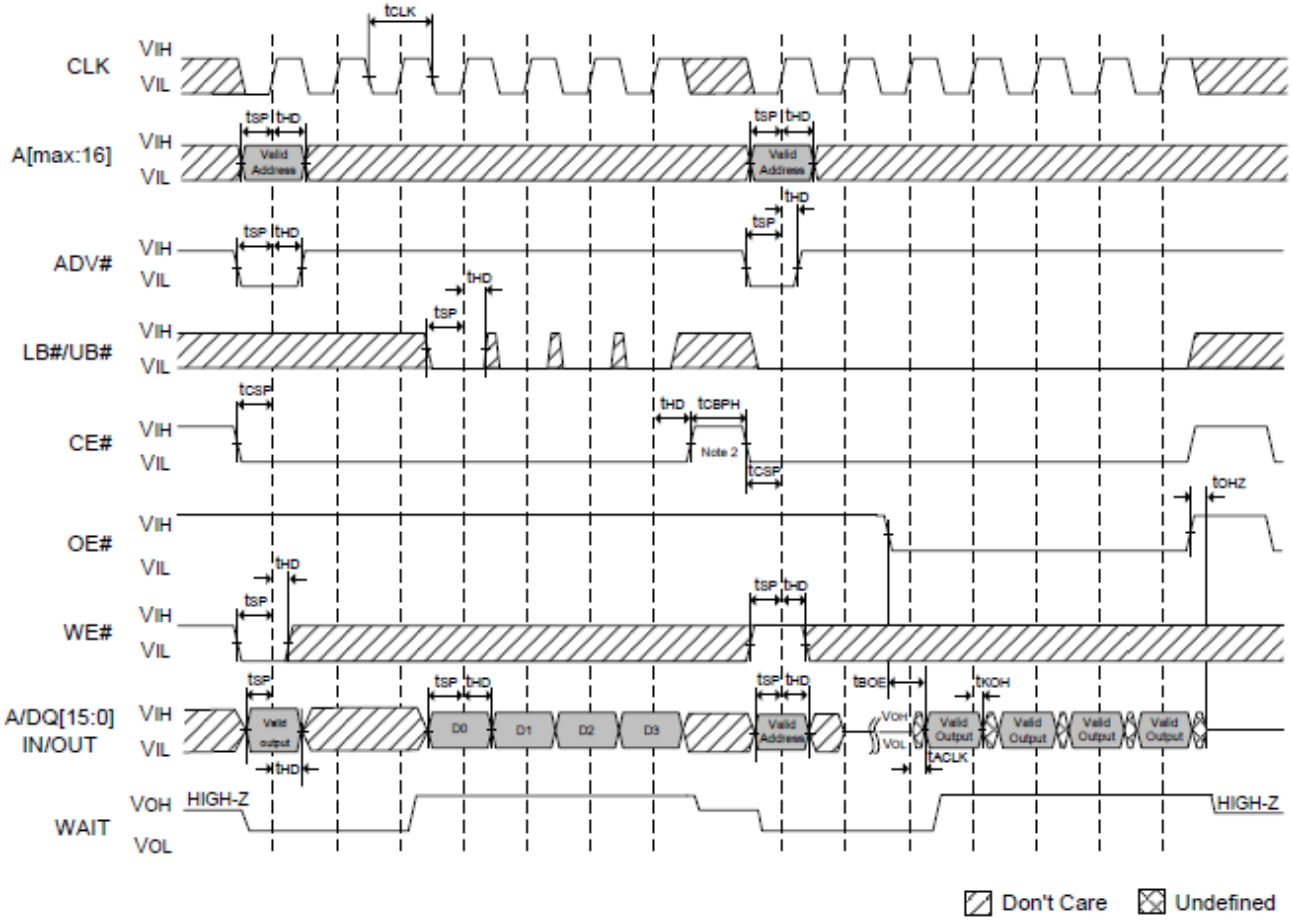
Figure 35: Burst WRITE Row Boundary Crossing



Notes:

1. Non-default BCR settings for burst WRITE at end of row: fixed or variable latency, WAIT active LOW, WAIT asserted during delay (shown as solid line).
2. WAIT will be asserted LC cycles for variable latency or fixed latency.

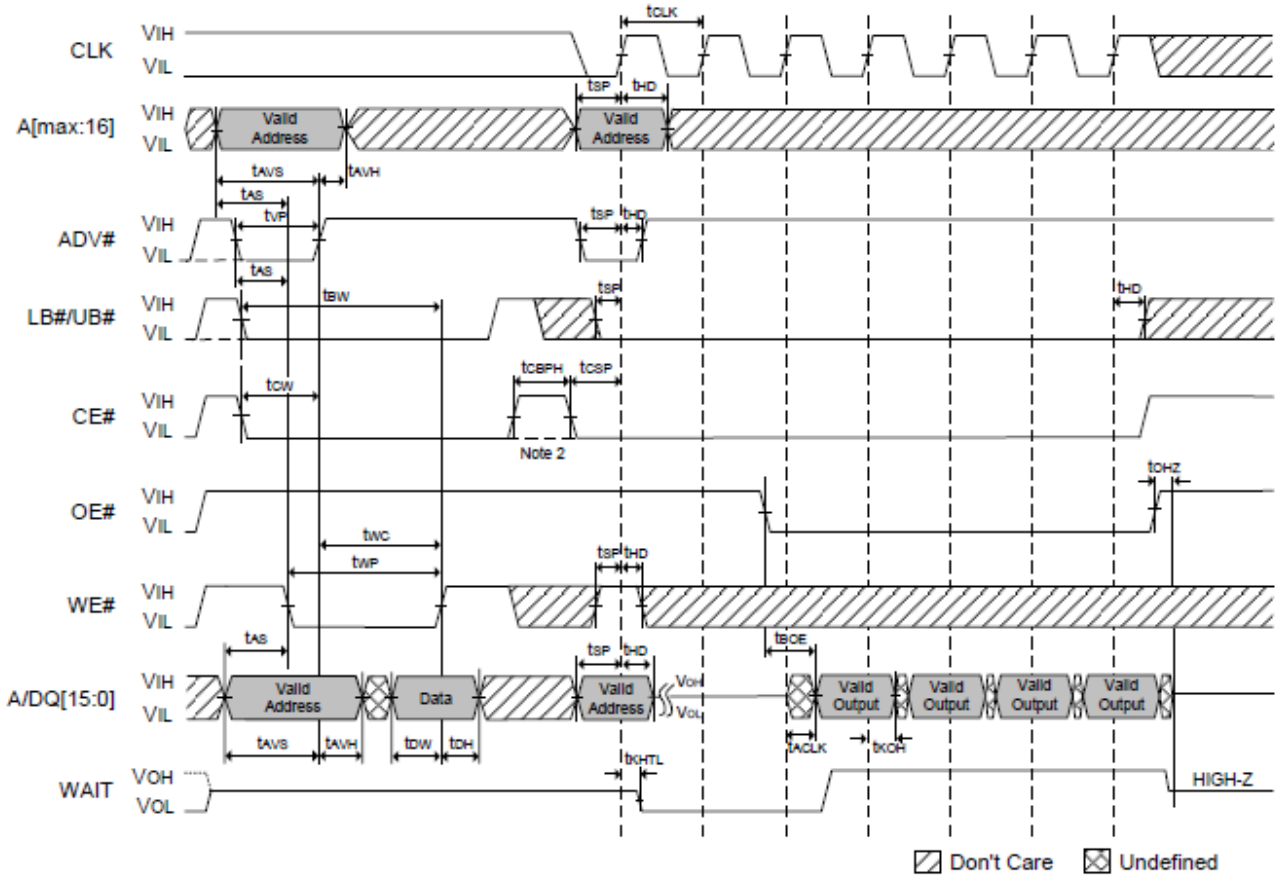
Figure 36: Burst WRITE Followed by Burst READ



Notes:

1. Non-default BCR settings for burst WRITE followed by burst READ: fixed or variable latency, latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.
2. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

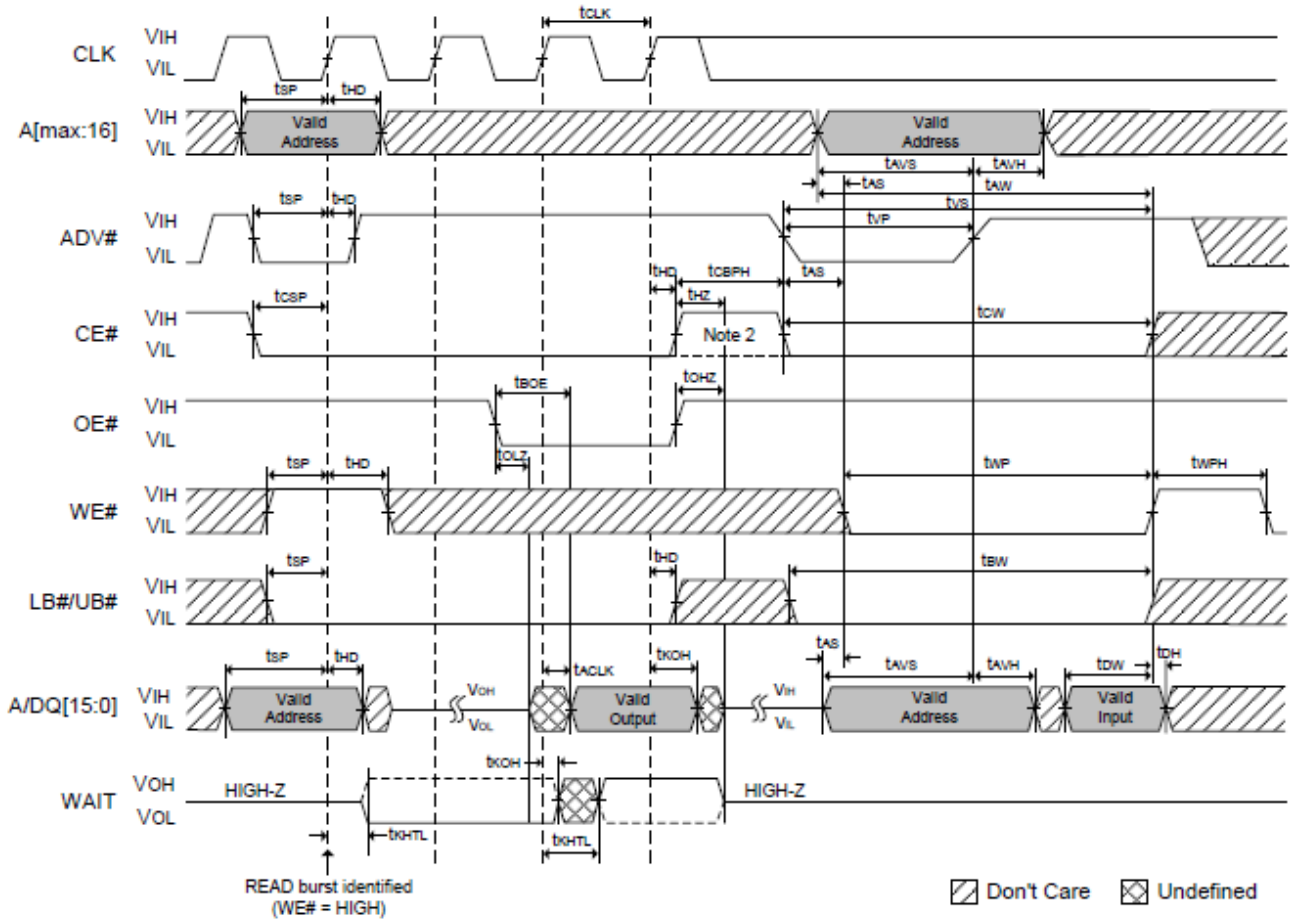
Figure 37: Asynchronous WRITE Followed by Burst READ



Notes:

1. Non-default BCR settings for asynchronous WRITE, with ADV# LOW, followed by burst READ: fixed or variable latency, latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.
2. When the device is transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when the device is transitioning to fixed latency burst READs. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

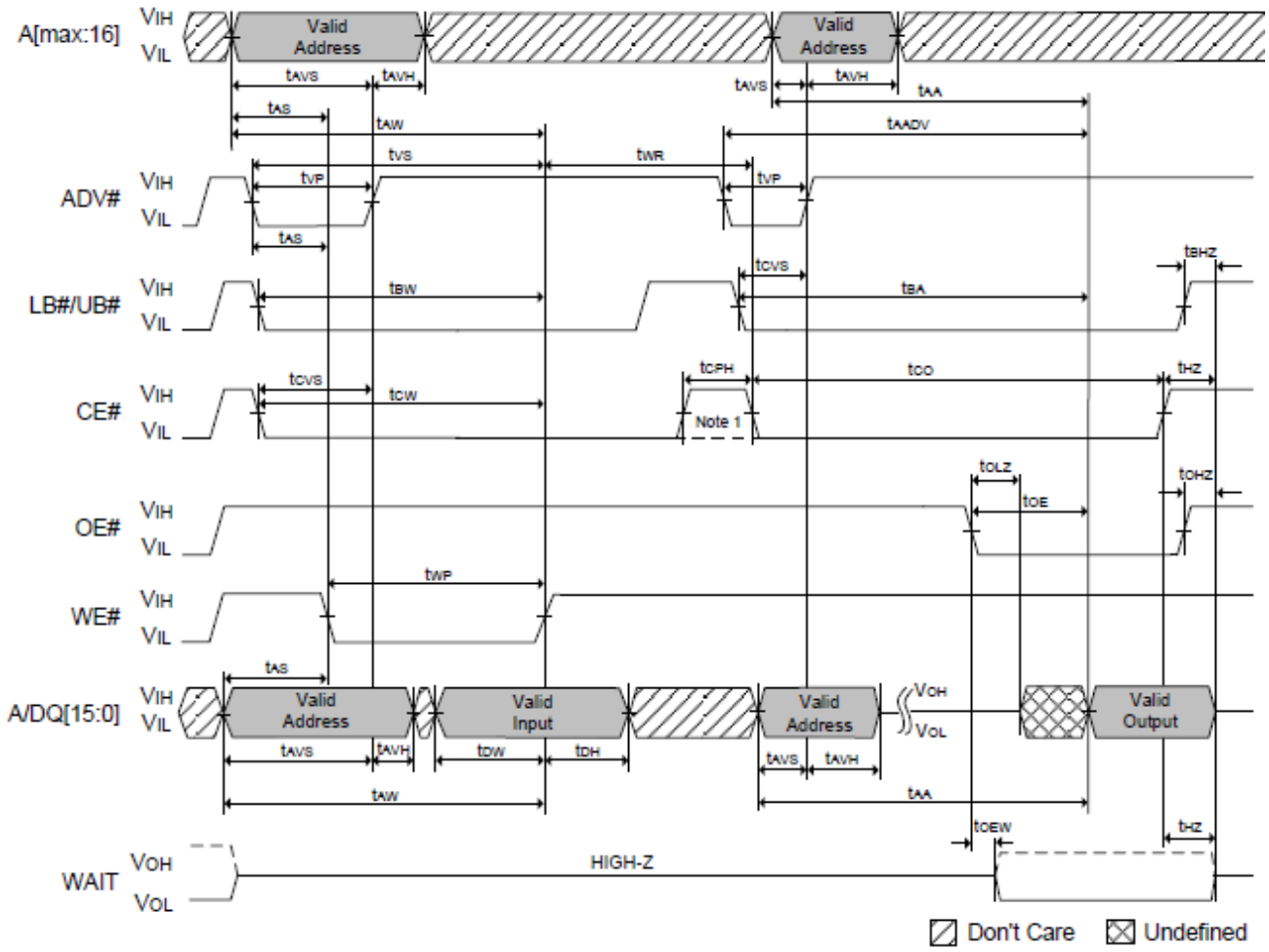
Figure 38: Burst READ Followed by Asynchronous WRITE



Notes:

1. Non-default BCR settings for burst READ followed by asynchronous WRITE using ADV#: fixed or variable latency, latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.
2. When the device is transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when the device is transitioning from fixed latency burst READs; asynchronous operation begins at the falling edge of ADV#. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

Figure 39: Asynchronous WRITE Followed by Asynchronous READ



Note:

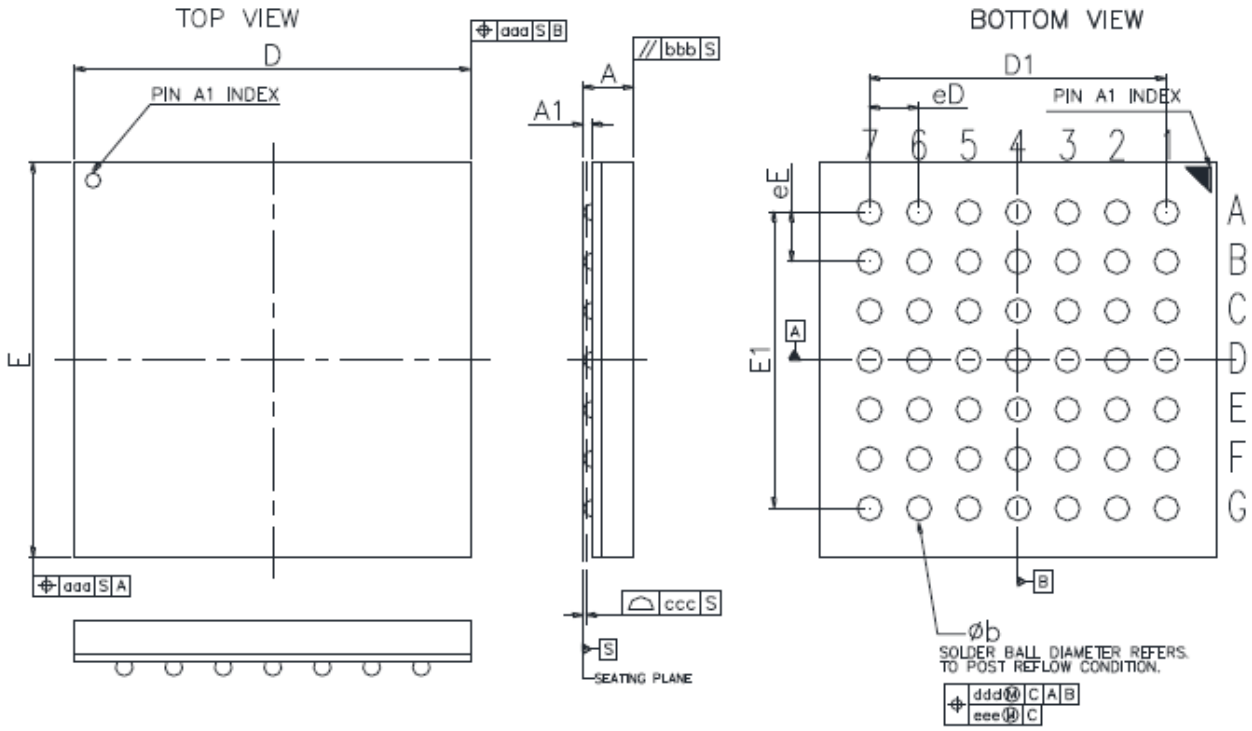
When configured for synchronous mode (BCR [15] = 0), CE# must remain HIGH for at least 5ns (tCPH) to schedule the appropriate refresh interval. Otherwise, tCPH is only required after CE#-controlled WRITEs.

6. ORDER INFORMATION

Part No.	VCC/VCCQ	I/O width	Package	Description
CS26LV64161Q8	1.8V/ 1.8V	16	49 TFBGA-4x4mm	CRAM ADMux, 133MHz, -40^{0}C~85^{0}C, DPD mode

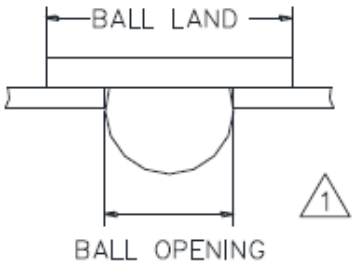
7. Package Outline

TFBGA 49 Balls (4x4 mm$_2$, Ball pitch: 0.5mm)



Controlling Dimension: Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.60	0.70	0.80	0.024	0.028	0.032
A1	0.13	0.18	0.23	0.005	0.007	0.009
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.90	4.00	4.10	0.154	0.158	0.161
E	3.90	4.00	4.10	0.154	0.158	0.161
D1	3.0 BSC.			0.118 BSC.		
E1	3.0 BSC.			0.118 BSC.		
eD	0.50 BSC.			0.020 BSC.		
eE	0.50 BSC.			0.020 BSC.		
aaa	--	--	0.15	--	--	0.006
bbb	--	--	0.20	--	--	0.008
ccc	--	--	0.10	--	--	0.004
ddd	--	--	0.15	--	--	0.006
eee	--	--	0.08	--	--	0.003



Note:
1. Ball land:0.34mm, Ball opening:0.24mm,
PCB Ball land suggested ≤0.24mm

mmm