Cover Sheet and Revision Status

版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20230012	Jul.14 -2023	New issue	Hank Lin

Chiplus reserves the right to change product or specification without notice.

Chiplus reserves the right to change product or specification without notice.

Chiplus reserves the right to change product or specification without notice.

Chiplus reserves the right to change product or specification without notice.

Chiplus reserves the right to change product or specification without notice.

Chiplus reserves the right to change product or specification without notice.

CS82xx

1Mb ~ 16Mb SPI MRAM

General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM). It features a SPI bus interface, XIP(execute-in-place) functionality, and hardware/software-based data protection mechanisms. SPI (Serial Peripheral Interface) is a synchronous serial communication interface with command, address and data signals.

It requires fewer pin counts than parallel interface and is easy to be configured on the system. The device is offered in density ranging from 1Mbit to 16Mbit. The device can replace Flash, FRAM or (nv)SRAM with same functionality and non-volatility.

The device provides various SPI modes to allow options for bandwidth expansion.

SSPI (Single SPI) modes has single(1) pin for command signals. And user can select an option for how many pins to be allocated to address and data signals among 1 pin, 2 pins or 4 pins.

DSPI (Dual SPI) modes provides dual(2) pins for command, address and data signals.

QSPI (Quad SPI) modes provides Quad(4) pins for command, address and data signals.

The device has nonvolatile register bits – status register, configuration register, serial number register, augmented 256 bytes and protection register for augment bytes. These register bits are required to be set at least once on power-up after high temperature solder reflow process.

The device is available in small footprint 8-pad WSON and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

Product Performance

Operation	Typical Values		Units
	1.8V	3.3V	
Frequency(SDR)	108 (Max.)		MHz
Frequency(DDR)	54 (Max.)		MHz
Standby Current	280	330	μA
Deep Power Down Current	25	80	μA
Active Read Current (4-4-4) SDR @108MHz	8	11	mA
Active Write Current (4-4-4) SDR @108MHz	21	24	mA

reserves the right to change product or specification without notice.

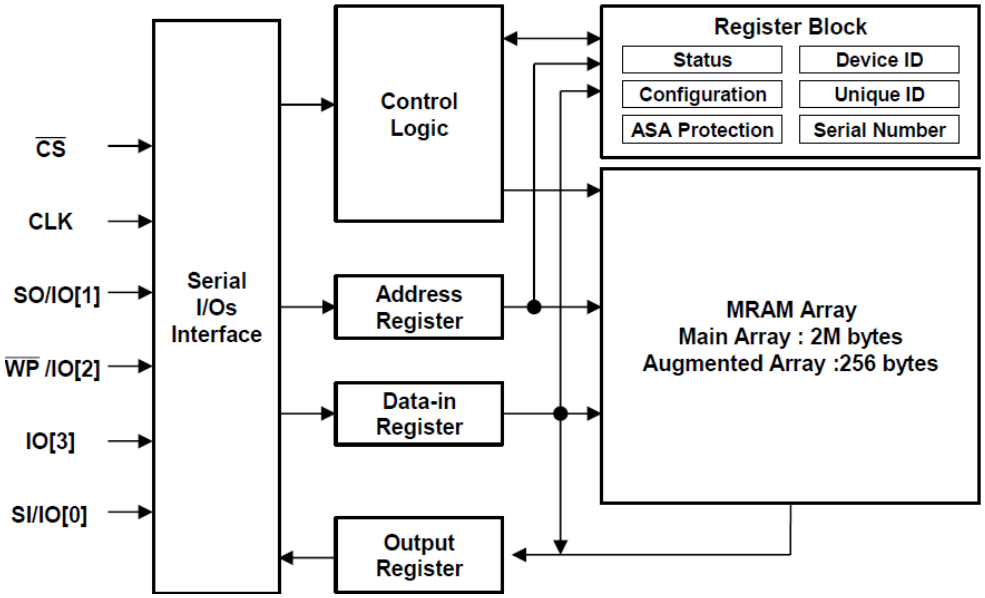
Features

- Supports Serial Peripheral Interface with Mode 0 and Mode 3 - Single SPI (1-1-1, 1-1-2, 1-2-2, 1-1-4, 1-4-4) - Dual SPI (2-2-2) - Quad SPI (4-4-4)
- Operating Frequency
  - Single Data Rates (SDR) : 108MHz
  - Double Data Rates (DDR) : 54MHz
- Supports XIP for read and write operations
- Fast write time and single byte writable
- Data protection
  - $\overline{WP}$ pin write protection
  - Block lock protection
- Nonvolatile status and configuration registers
- Identification
  - 64-bit unique ID
  - 64-bit serial number - user writable
- Augmented 256-byte nonvolatile-area
  - 8L WSON (5.0mm x 6.0mm)
  - 8L SOIC (150mil)
  - Read and write with user-protection
- Deep power down for low power
- Supports JEDEC reset
- Memory cell : STT-MRAM
- Density - 1Mb, 2Mb, 4Mb, 8Mb and 16Mb
- Data Integrity : No external ECC required
- Data Endurance
  - Unlimited read cycle
  - 10^{14} write cycles
- Data Retention
  - 10 years at 85°C
- Single Power Supply Operation
- Operating Temperature Range
  - Commercial Temperature : 0°C to 70°C
  - Industrial Temperature : -40°C to 85°C
- RoHS compliant packages

reserves the right to change product or specification without notice.

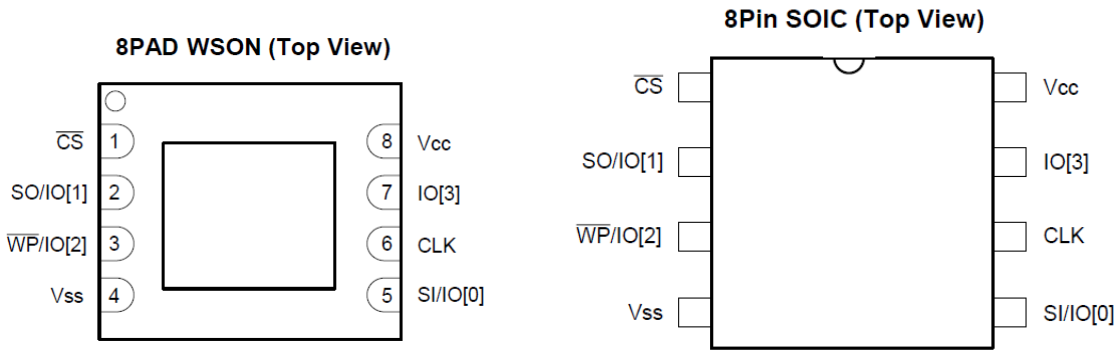
Function Block Diagram

Figure 1: Function Block Diagram



Package Pin Configuration

Figure 2: Pinout



reserves the right to change product or specification without notice.

Pin Descriptions

Table 1: Pin Description

Pin	Type	Description
$\overline{CS}$	Input	When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored, and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
CLK	Input	In SDR(single data rate) mode, command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In DDR(double data rate) mode command is latched on the rising edge of the clock and address and data inputs are latched on the rising and falling edges of the clock. Similarly, Data is output on both edges of the clock. The two SPI clock modes are supported as follows. ● SPI Mode 0 : SDR and DDR ● SPI Mode 3 : SDR only
$\overline{WP}$ /IO[2]	Input /Bidirectional	Write protects the status register in conjunction with the WREN bit (SR[1]) of the status register. The writing of status register is protected in related with $\overline{WP}$ and WPEN. See “Table 14 : Write Protection Modes”. This pin does not have internal pullups, it cannot be left floating and must be driven. $\overline{WP}$ is valid in Single SPI and Dual SPI mode. IO[2] : The bidirectional I/O in Quad SPI mode.
IO[3]	Bidirectional	IO[3] : The bidirectional I/O in Quad SPI modes.
SI/IO[0]	Input /Bidirectional	SI : The serial input in Single SPI mode. IO[0] : The bidirectional I/O in Dual and Quad SPI modes
SO/IO[1]	Output /Bidirectional	SO : The serial data output in Single SPI mode. IO[1] : The bidirectional in Dual and Quad SPI modes.
Vcc	Supply	Power pin
Vss	Supply	Ground pin

Power On/Off Sequence: 1.8V Device

- When power-up, power-down or power-loss, $\overline{CS}$ must follow Vcc to provide data protection.
- It is recommended that $\overline{CS}$ must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
- A 10KΩ pull-up resistor between Vcc and $\overline{CS}$ pin is recommended.
- Normal operation must start after t_{PU}.

reserves the right to change product or specification without notice.

Figure 3 : Power-up/down Behavior : 1.8V Device

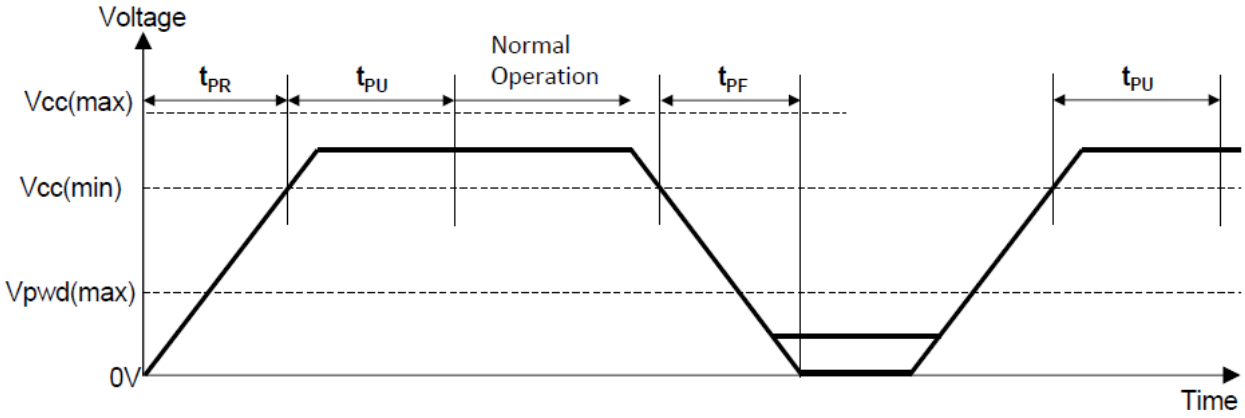


Table 2: Power Up/Down Timing – 1.8V Device

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	1.71	1.98	V
Vcc rising time	t_{PR}(1)	30	-	µs/V
Vcc falling time	t_{PF}(1)	30	-	µs/V
Vcc(min) to $\overline{CS}$ Low (first instruction) time	t_{PU}(1)	2.0	-	ms
Vcc needed to below Vpwd for ensuring initialization will occur	V_{PWD}(1)	-	0.8	V
Software Reset Time	t_{SRSE}(1)	2.0	-	ms

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

Power On/Off Sequence: 3.3V Device

- When power-up, power-down or power-loss, $\overline{CS}$ must follow Vcc to provide data protection.
- It is recommended that $\overline{CS}$ must follow Vcc when Vcc is below Vcc (minimum) and during t_{PU}.
- A 10KΩ pull-up resistor between Vcc and $\overline{CS}$ pin is recommended.
- Normal operation must start after t_{PU}.

reserves the right to change product or specification without notice.

Figure 3 : Power-up/down Behavior : 3.3V Device

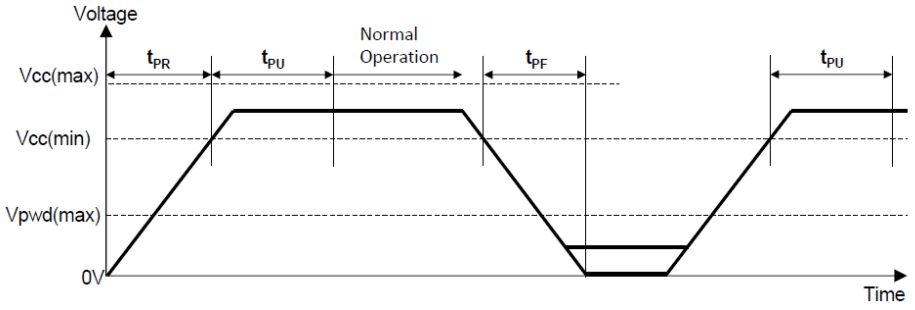


Table 3 : Power Up/Down Timing – 3.3V Device

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	2.7	3.6	V
Vcc rising time	$tPR^{(1)}$	30	-	µs/V
Vcc falling time	$tPF^{(1)}$	30	-	µs/V
Vcc(min) to $\overline{CS}$ Low (first instruction) time	$tPU^{(1)}$	2.0	-	ms
Vcc needed to below Vpwd for ensuring initialization will occur	$VPWD^{(1)}$	-	1.6	V

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

Memory Organization

Memory Map

Table 4: Memory Map

Density	Address Range		24-bit Address [23:0]	
1Mb	000000h – 01FFFFh		[23:17] – Logic '0'	[16:0] – Addressable
2Mb	000000h – 03FFFFh		[23:18] – Logic '0'	[17:0] – Addressable
4Mb	000000h – 07FFFFh		[23:19] – Logic '0'	[18:0] – Addressable
8Mb	000000h – 0FFFFFh		[23:20] – Logic '0'	[19:0] – Addressable
16Mb	000000h – 1FFFFFh		[23:21] – Logic '0'	[20:0] – Addressable

Augmented 256-Byte Area Map

Table 5 : Augmented 256-Byte Area Map

Density	Address Range	24-bit Address [23:0]	
1Mb~16Mb	000000h – 0000FFh1	[23:8] – Logic '0'	[7:0] - Addressable

Notes:

reserves the right to change product or specification without notice.

1: The augmented 256-byte area is divided into 8 individually readable and writeable sections (32 bytes per section). After an individual section is written, it can be written protected for each section to prevent further writing.

Register Address Map

The device provides the register read/write instructions to read and write data of each register. In addition, the device provides the register read and/or write function based on addresses by RDAR(65h) and WRAR(71h) commands.

Table 6 : Register Address

Register Name	Address
Status Register	0x000000h
Configuration Register 1	0x000002h
Configuration Register 2	0x000003h
Configuration Register 3	0x000004h
Configuration Register 4	0x000005h
Device Identification Register	0x000030h
Unique Identification Register	0x000040h
Serial Number Register	0x000080h

Notes:

1: Register address space is different from the memory array and augmented 256-byte area.

Instruction Command Set

Table 7: Control Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
No operation	NOOP	00	1-0-0, 2-0-0, 4-0-0		SDR			108MHz
Write Enable	WREN	06	1-0-0, 2-0-0, 4-0-0		SDR			108MHz
Write Disable	WRDI	04	1-0-0, 2-0-0, 4-0-0		SDR			108MHz
Enable DSPI	DPIE	37	1-0-0, 4-0-0		SDR			108MHz
Enable QSPI	QPIE	38	1-0-0, 2-0-0		SDR			108MHz
Enable SSPI	SPIE	FF	2-0-0, 4-0-0		SDR			108MHz
Enter Deep Power Down	DPDE	B9	1-0-0, 2-0-0, 4-0-0		SDR			108MHz
Exit Deep Power Down	DPDX	AB	1-0-0, 2-0-0, 4-0-0		SDR			108MHz
Software Reset Enable	SRTE	66	1-0-0, 2-0-0, 4-0-0		SDR			108MHz
Software Reset*	SRST	99	1-0-0, 2-0-0, 4-0-0		SDR			108MHz

reserves the right to change product or specification without notice.

Notes:

1: Software Reset (SRST) requires Software Reset Enable (SRTE) implemented in advance.

2: SSPI mode is enabled after power-on, software reset or JEDEC reset.

Table 8 : Read Register Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Read Status Register	RDSR	05	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Read Configuration Register 1	RDC1	35	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Read Configuration Register 2	RDC2	3F	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Read Configuration Register 3	RDC3	44	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Read Configuration Register 4	RDC4	45	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Read Configuration Register 1, 2, 3, 4	RDCX	46	1-0-1, 2-0-2, 4-0-4		SDR	4		108MHz
Read Device ID	RDID	9F	1-0-1, 2-0-2, 4-0-4		SDR	4		108MHz
Read Unique ID	RUID	4C	1-0-1, 2-0-2, 4-0-4		SDR	8		54MHz
Read Serial Number Register	RDSN	C3	1-0-1, 2-0-2, 4-0-4		SDR	8		108MHz
Read Augmented 256-byte Protection Register	RDAP	14	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Read Any Register - Address Based	RDAR	65	1-1-1, 2-2-2, 4-4-4		SDR	1,4,8	O	108MHz

Notes:

Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

Table 9 : Write Register Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Write Status Register	WRSR	01	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Write Configuration Registers 1, 2, 3, 4	WRCX	87	1-0-1, 2-0-2, 4-0-4		SDR	4		108MHz
Write Serial Number Register	WRSN	C2	1-0-1, 2-0-2, 4-0-4		SDR	8		108MHz
Write Augmented 256-byte Protection Register	WRAP	1A	1-0-1, 2-0-2, 4-0-4		SDR	1		108MHz
Write Any Register - Address Based	WRAR	71	1-1-1, 2-2-2, 4-4-4		SDR	1,8		108MHz

Notes:

reserves the right to change product or specification without notice.

1. Write Enable (WREN) should be implemented in advance of Write Register Instruction set regardless of CR4[1:0] setting.

2. The WREN prerequisite for write operation of memory array and augmented 256-byte area is described in Configuration Register 4.

Table 10 : Read Memory Array Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Read Memory Array - SDR	READ	03	1-1-1		SDR	1→∞		54MHz
Fast Read Memory Array - SDR	RDFT	0B	1-1-1, 2-2-2, 4-4-4	O	SDR	1→∞	O	108MHz
Fast Read Memory Array - DDR	DRFR	0D	1-1-1, 2-2-2, 4-4-4	O	DDR	1→∞	O	54MHz
Read Dual Output Memory Array - SDR	RDDO	3B	1-1-2	O	SDR	1→∞	O	108MHz
Read Dual Output Memory Array - DDR	DRDO	3D	1-1-2	O	DDR	1→∞	O	54MHz
Read Quad Output Memory Array - SDR	RDQO	6B	1-1-4	O	SDR	1→∞	O	108MHz
Read Quad Output Memory Array – DDR	DRQO	6D	1-1-4	O	DDR	1→∞	O	54MHz
Read Dual I/O Memory Read - SDR	RDDI	BB	1-2-2	O	SDR	1→∞	O	108MHz
Read Dual I/O Memory Read - DDR	DRDI	BD	1-2-2	O	DDR	1→∞	O	54MHz
Read Quad I/O Memory Read - SDR	RDQI	EB	1-4-4	O	SDR	1→∞	O	108MHz
Read Quad I/O Memory Read - DDR	DRQI	ED	1-4-4	O	DDR	1→∞	O	54MHz

Notes:

1: Read Instruction must include Latency cycles to meet operating frequency.

2: Latency is configurable through Configuration Register 2 (CR2[3:0]) and frequency dependent.

Required latency is described in Configuration Register 2.

Table 11 : Write Memory Array Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Write Memory Array - SDR	WRTE	02	1-1-1		SDR	1→∞		108MHz
Fast Write Memory Array - SDR	WRFT	DA	1-1-1, 2-2-2, 4-4-4	O	SDR	1→∞		108MHz
Fast Write Memory Array - DDR	DRFW	DE	1-1-1, 2-2-2, 4-4-4	O	DDR	1→∞		54MHz

reserves the right to change product or specification without notice.

Write Dual Input Memory Array- SDR	WDUI	A2	1-1-2	O	SDR	1→∞		108MHz
Write Dual Input Memory Array– DDR	DWUI	A4	1-1-2	O	DDR	1→∞		54MHz
Write Quad Input Memory Array- SDR	WQDI	32	1-1-4	O	SDR	1→∞		108MHz
Write Quad Input Memory Array- DDR	DWQI	31	1-1-4	O	DDR	1→∞		54MHz
Write Dual I/O Memory Array - SDR	WDIO	A1	1-2-2	O	SDR	1→∞		108MHz
Write Dual I/O Memory Array -DDR	DWIO	A3	1-2-2	O	DDR	1→∞		54MHz
Write Quad I/O Memory Array - SDR	WQIO	D2	1-4-4	O	SDR	1→∞		108MHz
Write Quad I/O Memory Array - DDR	DWQO	D1	1-4-4	O	DDR	1→∞		54MHz

Notes:

1: Write Enable (WREN) for array writing is configurable (Configuration Register 4 – CR4[1:0])

Table 12 : Augmented 256-Byte Area Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Read Augmented 256-Byte Area - SDR	RDAS	4B	1-1-1		SDR	1→256	O	108MHz
Write Augmented 256-Byte Area - SDR	WRAS	42	1-1-1		SDR	1→256		108MHz

Notes:

1: The address bits ADDR[23:8] must be Logic '0' for this Instruction.

1: Write Enable (WREN) for array writing is configurable (Configuration Register 4 – CR4[1:0])

Register Description

Status Register / Device Protection Register

The device offers both hardware and software-based data protection schemes. Hardware protection is through $\overline{WP}$ pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array. Status Register contains options for enabling/disabling data protection. By controlling configuration bits in Status Register, use can protect data in memory array based on software protection schemes.

reserves the right to change product or specification without notice.

Table 13 : Status Register-Data Protection

Bits	Name	Read/ Write	Default State	Description
SR[7]	WPEN	R/W	-	Hardware Based $\overline{WP}$ Protect Bit 1: Protection Enabled – write protects when $\overline{WP}$ is Low 0: Protection Disabled – Doesn't write protect when $\overline{WP}$ is Low
SR[6]	SNPEN	R/W	-	Serial Number Protect Bit 1: Serial Number Write protected 0: Serial Number Writable
SR[5]	TB	R/W	-	Top/Bottom Memory Array Protect Selection 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BP[2]	R/W	-	Block Protection Bits
SR[3]	BP[1]	R/W	-	
SR[2]	BP[0]	R/W	-	
SR[1]	WREN	R	0	Write Protection Enable 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	R	-	Reserved for future use

Note : SR[7:2] are nonvolatile bits.

Write Protection Modes

WPEN bit ($SR_{[7]}$) is used in conjunction with the WREN bit (SR[1]) and the $\overline{WP}$ pin to provide hardware block protection. $SR_{[7:2]}$ will remain set from the nonvolatile registers whenever the power is on. The WREN bit is volatile and set "1" by the Write Enable command. It is set to "0" at power up. The device enters hardware protection when the $\overline{WP}$ input is low and the Status Register WPEN bit is set to 1, and the status and configuration register bits cannot be changed. The device exits from hardware protection when the /WP pin goes high or WPEN bit is set to 0, and the register bits can be changed.

Table 14 : Write Protection Modes

WREN	WPEN	$\overline{WP}$ (Pin)	Status & Configuration Registers	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	0	Protected	Protected	Unprotected
1	1	1	Unprotected	Protected	Unprotected

Notes:

reserves the right to change product or specification without notice.

1: Memory address range protection based on Block Protection Bits

2. X: Don't Care – Can be Logic '0' or '1'

3. Protected: Write protected, Unprotected: Writable

Block Protection Modes

The write protection blocks for the memory array are determined by the status register bits (TB and BP[2:0]) as Table 15. TB and BP[2:0] can be modified by WRSR command when the $\overline{WP}$ input is high or the Status Register WPEN bit is set to 0, and MAPLK(CR1[2]) is set to 0.

Table 15 : Block Protection Address Range Selection

TB	BP[2]	BP[1]	BP[0]	Protected Portion	1Mb	2Mb	4Mb	8Mb	16Mb
0/1	0	0	0	None	None	None	None	None	None
0	0	0	1	Upper 1/64	01F800h – 01FFFFh	03F000h – 03FFFFh	07E000h – 07FFFFh	0FC000h – 0FFFFFh	1F8000h – 1FFFFFh
0	0	1	0	Upper 1/32	01F000h – 01FFFFh	03E000h – 03FFFFh	07C000h – 07FFFFh	0F8000h – 0FFFFFh	1F0000h – 1FFFFFh
0	0	1	1	Upper 1/16	01E000h – 01FFFFh	03C000h – 03FFFFh	078000h – 07FFFFh	0F0000h – 0FFFFFh	1E0000h – 1FFFFFh
0	1	0	0	Upper 1/8	01C000h – 01FFFFh	038000h – 03FFFFh	070000h – 07FFFFh	0E0000h – 0FFFFFh	1C0000h – 1FFFFFh
0	1	0	1	Upper 1/4	018000h – 01FFFFh	030000h – 03FFFFh	060000h – 07FFFFh	0C0000h – 0FFFFFh	180000h – 1FFFFFh
0	1	1	0	Upper 1/2	010000h – 01FFFFh	020000h – 03FFFFh	040000h – 07FFFFh	080000h – 0FFFFFh	100000h – 1FFFFFh
1	0	0	1	Lower 1/64	000000h – 0007FFh	000000h – 000FFFh	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh
1	0	1	0	Lower 1/32	000000h – 000FFFh	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh
1	0	1	1	Lower 1/16	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh
1	1	0	0	Lower 1/8	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh
1	1	0	1	Lower 1/4	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh
1	1	1	0	Lower 1/2	000000h –	000000h –	000000h –	000000h –	000000h –

reserves the right to change product or specification without notice.

					00FFFFh	01FFFFh	03FFFFh	07FFFFh	0FFFFFh
0/1	1	1	1	All	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh

Augmented 256-Byte Area Protection

Augmented 256-Byte Area Protection register contains options for enabling/disabling data protection for eight 32-byte sections.

Table 16 : Augmented 256-Byte Area Protection Register – Read and Write

Bits	Name	Address Range	Read/ Write	Default State	Description
ASP[7]	ASPS[7]	0000E0h – 0000FFh	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	0000C0h – 0000DFh	R/W	0	
ASP[5]	ASPS[5]	0000A0h – 0000BFh	R/W	0	
ASP[4]	ASPS[4]	000080h – 00009Fh	R/W	0	
ASP[3]	ASPS[3]	000060h – 00007Fh	R/W	0	
ASP[2]	ASPS[2]	000040h – 00005Fh	R/W	0	
ASP[1]	ASPS[1]	000020h – 00003Fh	R/W	0	
ASP[0]	ASPS[0]	000000h – 00001Fh	R/W	0	

Note : ASP[7:0] are nonvolatile bits.

Configuration Register 1 (Read/Write)

Configuration Register 1 controls locking/unlocking data protection options set in the Status register.

Once locked, the protection options cannot be changed in the Status register.

Table 17 : Configuration Register 1 – Read and Write

Bits	Name	Read/ Write	Default State	Selection Options
CR1[7]	RSVD	R/W	-	Reserved for future use
CR1[6]	RSVD	R/W	-	Reserved for future use
CR1[5]	RSVD	R/W	-	Reserved for future use
CR1[4]	RSVD	R/W	-	Reserved for future use
CR1[3]	RSVD	R/W	-	Reserved for future use
CR1[2]	MAPLK	R/W	-	Status Register TB, BP[2:0] Protect 1: Lock TB and BP[2:0] 0: Unlock TB and BP[2:0]

reserves the right to change product or specification without notice.

CR1[1]	RSVD	R/W	-	Reserved for future use
CR1[0]	ASPLK	R/W	-	Augmented 256-Byte Area Data Protection 1: Write Protection for Augmented Area Data regardless of ASP[7:0] 0: Write Protection for Augmented Area Data depending on ASP[7:0]

Note : CR1[7:0] are nonvolatile bits.

Configuration Register 2 (Read/Write)

Configuration Register 2 controls the interface type along with memory array access latency.

Table 18 : Configuration Register 2 – Read and Write

Bits	Name	Read/ Write	Default State	Description
CR2[7]	RSVD	R/W	-	Reserved for future use
CR2[6]	QPIEN	R	0	Quad SPI (QPI 4-4-4) Interface Mode 1: Quad SPI (QPI 4-4-4) Enabled 0: Single SPI (SPI 1-X-X) Enabled
CR2[5]	RSVD	R/W	-	Reserved for future use
CR2[4]	DPIEN	R	0	Dual SPI (DPI 2-2-2) Interface Mode 1: Dual SPI (DPI 2-2-2) Enabled 0: Single SPI (SPI 1-X-X) Enabled
CR2[3]	RL[3]	R/W	-	Read Latency Selection Bits : CR2[3:0] 0000: 0 Cycle 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycles 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	RL[2]		-	
CR2[1]	RL[1]		-	
CR2[0]	RL[0]		-	

Notes:

reserves the right to change product or specification without notice.

1. Read Latency is frequency dependent.

2. Read(03h) does not depend on Read latency Selection Bits, CR2[3:0].

3. CR2[7,5,3:0] are nonvolatile bits.

Table 19 : Read Latency Cycles vs. Maximum Frequency (Memory Area)

Read Type	Data Rate	XIP	Latency Cycles	Max Frequency
1-1-1 (READ 03h)	SDR	-	0	54MHz
1-1-1, 1-1-2, 1-2-2, 2-2-2, 1-1-4, 1-4-4, 4-4-4	SDR	O	6-15	108MHz
1-1-1, 1-1-2, 1-2-2, 2-2-2, 1-1-4, 1-4-4, 4-4-4	DDR			54MHz

Notes:

Read(03h) does not depend on Read latency Selection Bits, CR2[3:0]. The latency of Read(03h) is always 0-cycle

Table 20 : Read Latency Cycles vs. Maximum Frequency (Augmented 256-Byte Area)

Read Type	Data Rate	XIP	Latency Cycles	Max Frequency
1-1-1 (RDAS 4Bh)	SDR	-	6-15	54MHz
1-1-1 (RDAS 4Bh)	SDR	-	8-15	108MHz

Table 21 : Latency Cycles vs. Maximum Frequency (Read Any Register Instruction)

Read Type	Data Rate	XIP	Latency Cycles	Max Frequency
1-1-1 (RDAR 65h)	SDR	-	8	108MHz
2-2-2 (RDAR 65h)	SDR	-	4	108MHz
4-4-4 (RDAR 65h)	SDR	-	2	108MHz

Notes:

1. RDAR(65h, read any register instruction) does not depend on Read latency Selection Bits, CR2$_{[3:0]}$.

reserves the right to change product or specification without notice.

Configuration Register 3 (Read/Write)

Configuration Register 3 controls the output driver strength along with the boundary size of read data wrapping.

Table 22 : Configuration Register 3 – Read and Write

Bits	Name	Read/ Write	Description
CR3[7]	DRV[2]	R/W	Output Driver Strength Selection DRV[2:0] 3.3V 1.8V 000: 36Ω 35Ω 001: 100Ω 95Ω 010: 75Ω 63Ω 011: 60Ω 50Ω 100: 48Ω 40Ω 101: 41Ω 30Ω 110: 29Ω 26Ω 111: 24Ω 22Ω
CR3[6]	DRV[1]		
CR3[5]	DRV[0]		
CR3[4]	WRPEN	R/W	Read WRAP Enable 1: Read Wrap Enabled 0: Read Wrap Disabled
CR3[3]	RSVD	R/W	Reserved for future use
CR3[2]	WRPL[2]	R/W	Wrap length configuration WRPL[2:0] 000: 16-byte wrap 001: 32-byte wrap 010: 64-byte wrap 011: 128-byte wrap 100: 256-byte wrap 101: 512-byte wrap 110: 1K-byte wrap 111: Reserved
CR3[1]	WRPL[1]		
CR3[0]	WRPL[0]		

Notes:

Default output strength is DRV[2:0]=000.

CR3[7:0] are nonvolatile bits.

reserves the right to change product or specification without notice.

	Description
WRPEN(CR3[4]) =Low	Read and write operation : continuous mode Read or write operation starts at the input address, and once the address reaches the maximum address boundary, it automatically returns to minimum address(000000h) until $\overline{CS}$ goes to high.
WRPEN(CR3[4]) =High	Read operations : wrap mode Read wrap mode is enabled when WRPEN(CR3[4]) is High, and the read data wrap length is controlled by WRPL[2:0]. The output data starts at the input address, data are output sequentially. Once it reaches the ending boundary, the output will wrap around to the beginning boundary automatically until $\overline{CS}$ is pulled high. Write operation : continuous mode Write operation starts at the input address, and once the address reaches the maximum address boundary, it automatically returns to minimum address(000000h) until $\overline{CS}$ goes to high.

Configuration Register 4 (Read/Write)

Configuration Register 4 controls Write Enable protection (WREN – Status Register) reset functionality during memory array writing1. This functionality makes SPI MRAM compatible to other SPI devices.

Table 23 : Configuration Register 4 – Read and Write

Bits	Name	Read/ Write	Default State	Selection Options
CR4[7:2]	RSVD	R/W	-	Reserved for future use
CR4[1]	WRENS[1]		-	**00:** Normal: WREN is prerequisite to all Memory Array and Augmented 256-byte Area Write instruction. (WREN is reset after $\overline{CS}$ goes High) **01:** SRAM: WREN is not a prerequisite to Memory Array and Augmented 256-byte Area Write instruction (WREN is ignored)
CR4[0]	WRENS[0]		-	**10:** Back-to-Back: WREN is prerequisite to only the first Memory Array Write or Augmented 256-byte Area instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset after $\overline{CS}$ goes High) **11:** Reserved

Notes:

1. Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 4 settings. In other words, all register write Instructions require WREN to be set and WREN resets once $\overline{CS}$ goes High for the write instruction. CR4[1:0] only affects the writing for

reserves the right to change product or specification without notice.

memory and augmented 256-bytes area.

2. CR4[7:0] are nonvolatile bits.

Device Identification Register (Read Only)

Device identification register contains Manufacturing ID along with device configuration information.

Table 24 : Device Identification Register – Read Only

Bits	Manufacturer ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temperature	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1101 1001	0000 : QSPI	0001 : 3.3V 0010 : 1.8V	0000 : -40ºC~85ºC	0001 : 1Mb 0010 : 2Mb 0011 : 4Mb 0100 : 8Mb 0101 : 16Mb	00000001 : 108MHz

Serial Number Register (Read/Write)

The device provides 64-bits Serial Number register and the user can write it.

Table 25 : Serial Number Register – Read and Write

Bits	Name	Description	Read/ Write	State
SN[63:0]	SN	Serial Number Value	R/W	User writable

Notes:

1: Serial Number Bits are non-volatile, and user should write the data after solder reflow process.

Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

reserves the right to change product or specification without notice.

Table 26 : Unique ID Register – Read Only

Bits	Name	Description	Read/ Write	Selection Options
UID[63:0]	UID	Unique Identification Number Value	R	Value stored is written in the factory and is device specific

Device Operation

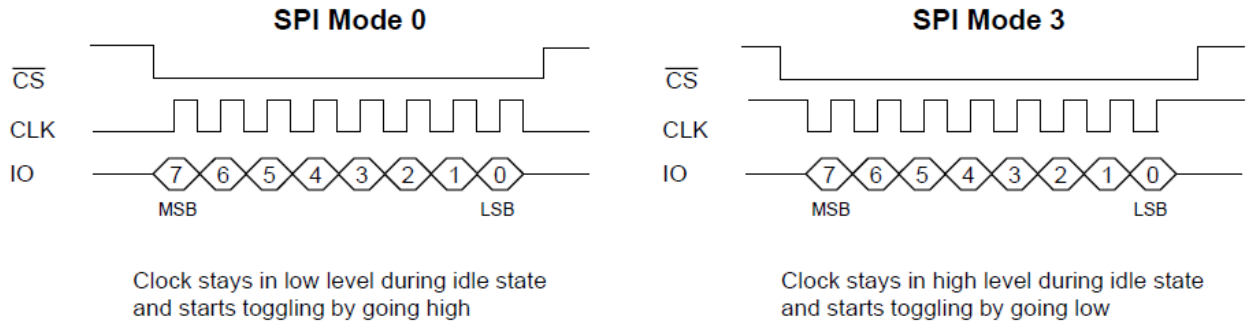
General Operation

Before an instruction is issued, status register should be checked to ensure device is ready for the intended operation. When correct command is input to this device, it enters active mode and remains in active mode until next $\overline{CS}$ rising edge.
Do not enter an invalid opcode(except instruction set). When $\overline{CS}$ goes to high, the device enters standby mode. All communication between a host and the device is in the form of commands. commands define the operation that must be executed. Instruction consists of a command followed by an optional address modifier and data transferred. All command, address and data information are transferred sequentially.

SPI Clock Modes

- The following two SPI clock modes are supported.
  - SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR
  - SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only

Figure 5 : SPI Clock Modes



SPI Interface Modes

- The device supports 3 categories of SPI interface modes.
  - Single SPI (SSPI) : command is transferred through one I/O pin.

reserves the right to change product or specification without notice.

1) Address and data are transferred through one pin

2) Address is transferred through one pin, data is transferred through two pins

3) Address is transferred through one pin, data is transferred through four pins

4) Address and data are transferred through two pins

5) Address and data are transferred through four pins

- Dual SPI (DSPI) : All command, address and data are transferred through two I/O pins.
- Quad SPI (QSPI) modes : All command, address and data are transferred through four I/O pins.

- Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 1-4-4 represents command being sent on a single I/O (SI / IO[0]) and address/data being sent on four I/Os (IO[3:0]).

Table 27 : Pin Assignment / Interface Modes

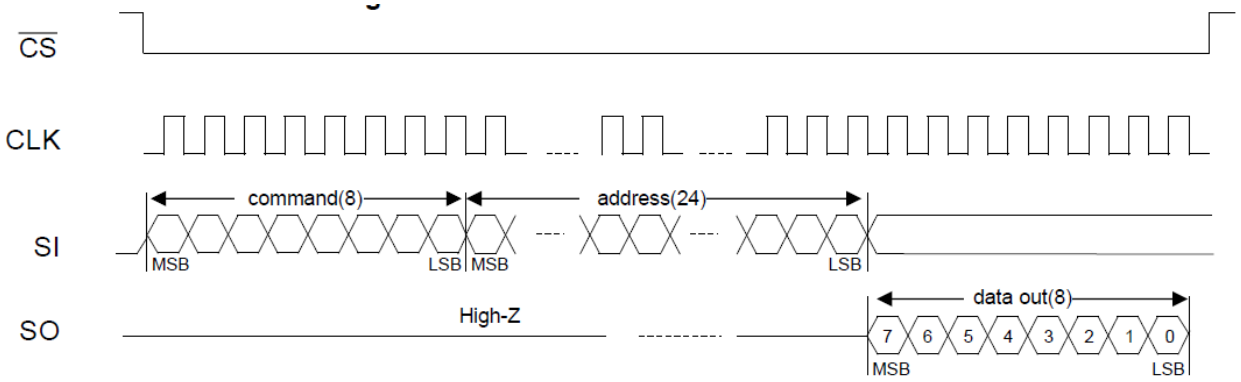
Instruction Component	Interface Modes (Command-Address-Data)						
	SSPI 1-1-1	SSPI 1-1-2	SSPI 1-2-2	DSPI 2-2-2	SSPI 1-1-4	SSPI 1-4-4	QSPI 4-4-4
Command	SI/IO[0]	SI/IO[0]	SI/IO[0]	IO[1:0]	SI/IO[0]	SI/IO[0]	IO[3:0]
Address	SI/IO[0]	SI/IO[0]	IO[1:0]	IO[1:0]	SI/IO[0]	IO[3:0]	IO[3:0]
Data Input	SI/IO[0]	IO[1:0]	IO[1:0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]
Data Output	SO/IO[1]	IO[1:0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[3:0]

MSB/LSB Location in data bits

The most significant bit(MSB) is placed first at all commands, address and data.

reserves the right to change product or specification without notice.

Figure 6 : Location of MSB and LSB



For Dual SPI and Quad SPI, the order of data bits is alternately decided among the IO pins.

Figure 7 : MSB and LSB in DSPI and QSPI

Note;

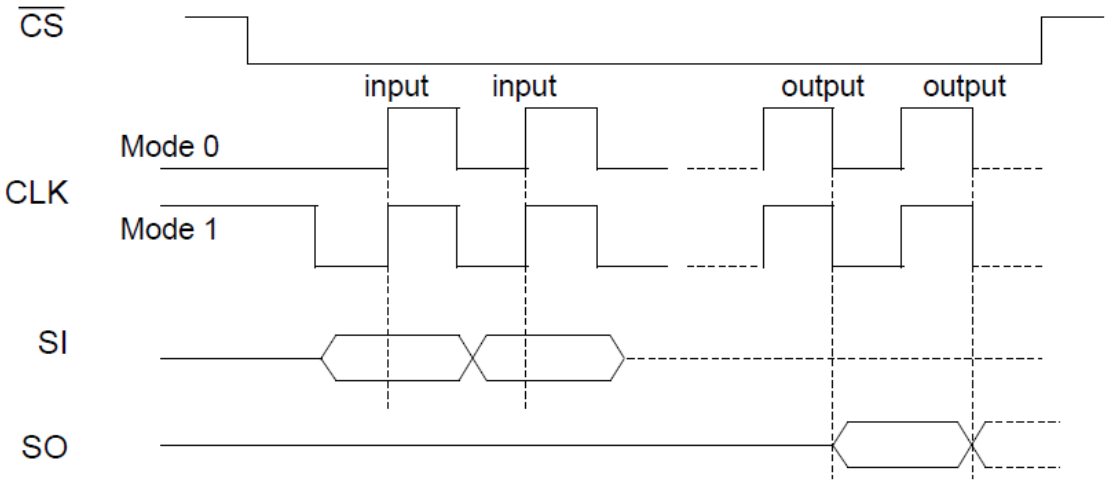
All commands, Address, XIP and Data follow this order.

Data Rate (SDR/DDR)

In Single Data Rate mode (SDR), command, address and data inputs are latched on the rising edge of the clock. Data is outputted on the falling edge of the clock.

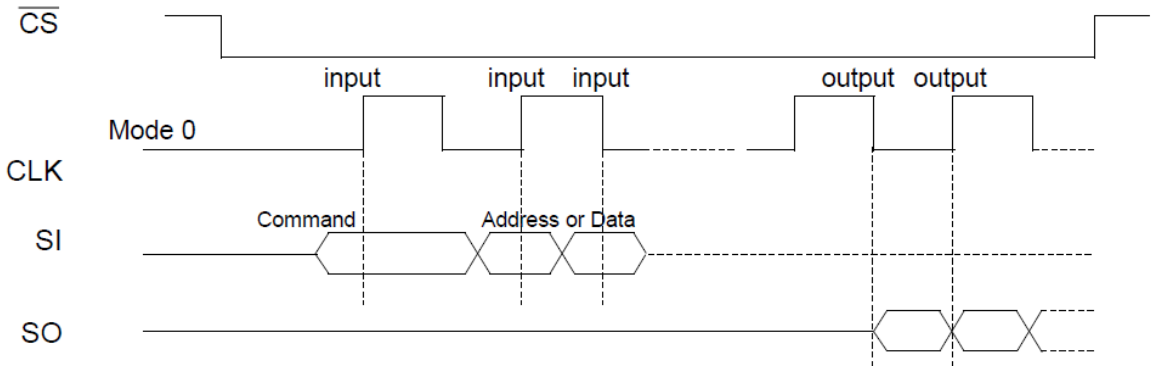
reserves the right to change product or specification without notice.

Figure 8 : Description of SDR Instruction Type



In Double Data Rate mode (DDR), command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Data is output on both edges of the clock.

Figure 9 : Description of DDR Instruction Type



Instruction Structure

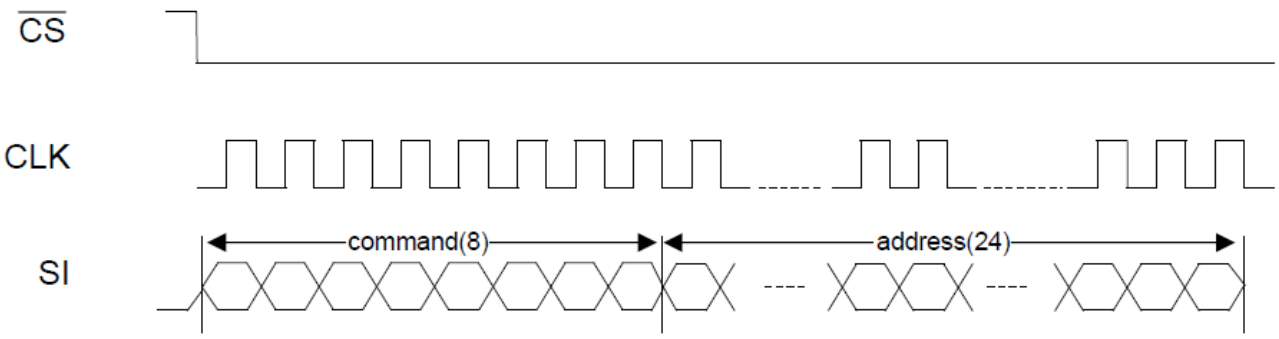
Each instruction starts out with an 8-bit command. The command selects the type of operation.

The instruction can be stand alone or followed by address to select a memory location or register.

The address is always 24-bits wide.

reserves the right to change product or specification without notice.

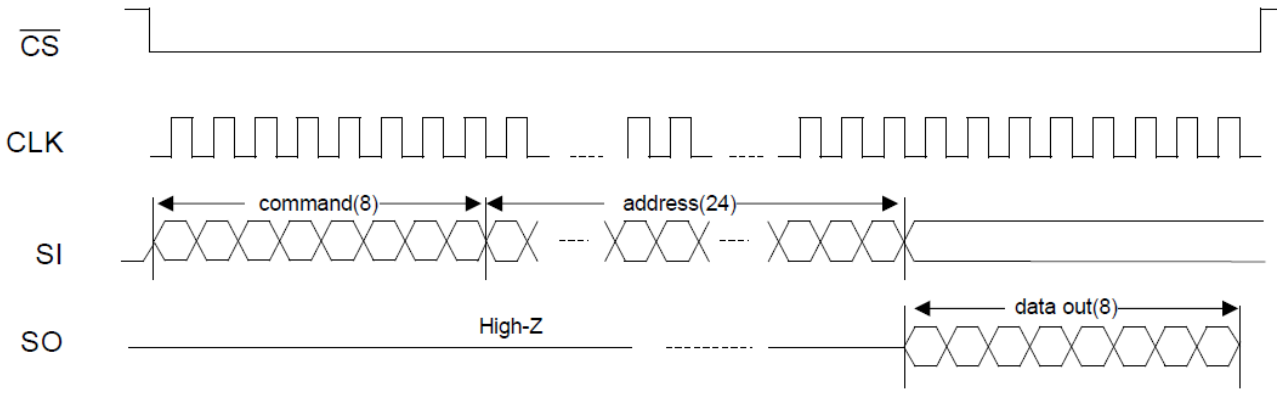
Figure 10 : Description of command followed by Address (SSIP mode)



Read Operation

Read operation starts from pulling $\overline{CS}$ Low. 8 bits Read command(03h) is transmitted to the device then 24 bit address is following while the first 7 MSB bits of address are don't care. The device outputs the data at selected address to the SO pin. The read operation can be terminated by pulling $\overline{CS}$ high.

Figure 11 : Description of Read Operation (SSIP mode)

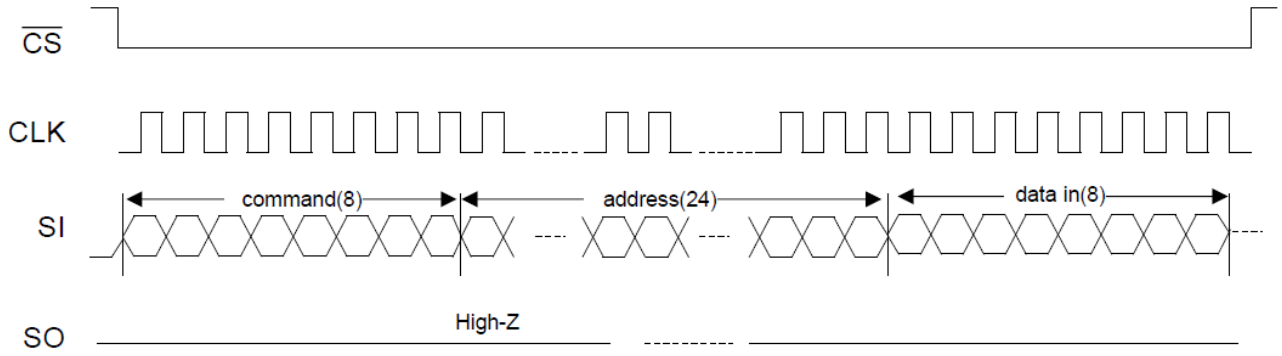


Write Operation

Write operation starts from pulling $\overline{CS}$ Low. 8 bits Write command(02h) is transmitted to the device then 24 bit address is following while the first 7 MSB bits of address are don't care. The data on the SI pin is written to the device at selected address. The write operation can be terminated by pulling $\overline{CS}$ high.

reserves the right to change product or specification without notice.

Figure12 : Description of Write Operation (SSPI mode)



Note :

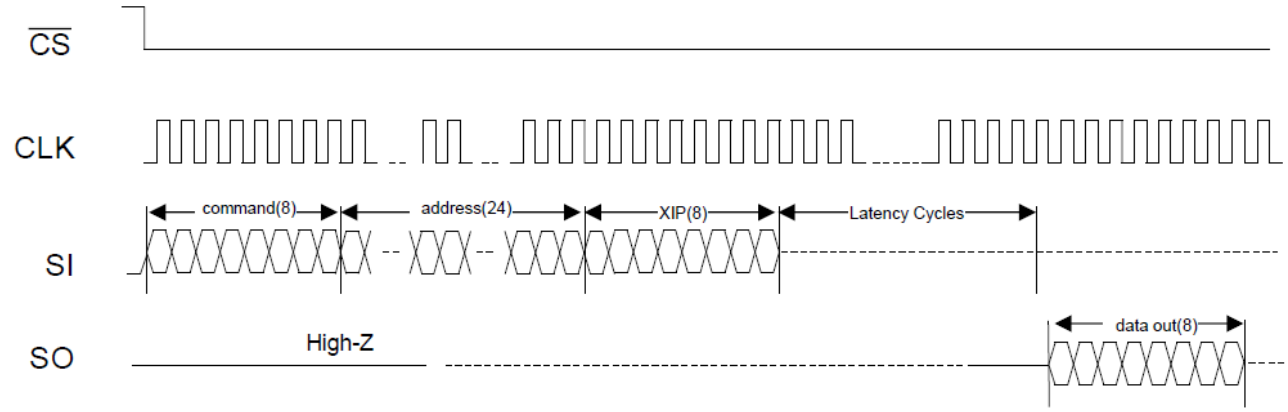
In normal operational mode, write instructions must be preceded by the WREN command. WREN command sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI command.

The device offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array or the augmented 256-byte area. These modes are set in Configuration Register 4.

XIP (Execute in Place) Operation

For read and write operation, the device offers XIP (execute in place) mode. XIP allows a series of read or write operation without loading individual read or write command for each instruction, which results in reduced random-access time. XIP is enabled by entering byte AXh and disabled by entering any byte not equal to AXh. These respective bytes must be entered following the address bits. Read operation with XIP needs extra Read-Latency before data coming out from SO pin. The latencies are specified in Table 19 : Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP) .

Figure 13 : Description of Read Operation with XIP (SSIP mode)



reserves the right to change product or specification without notice.

Continuing Read/Write

The entire memory array can be read from or written to using a single read or write instruction. After the starting address is entered, subsequent address is internally incremented as long as $\overline{CS}$ is Low and CLK continues toggling.

Figure 14 : Description of Continuing Read Operation (SSIP mode)

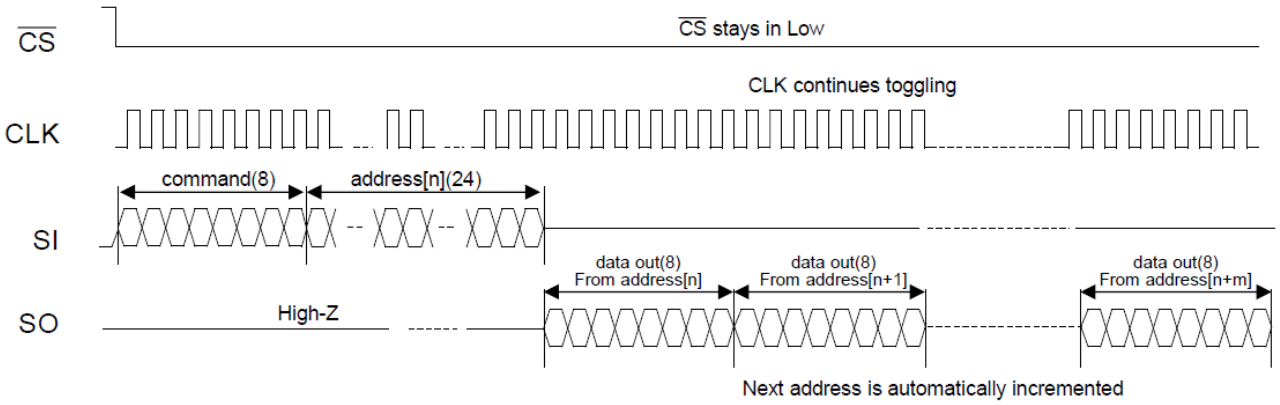
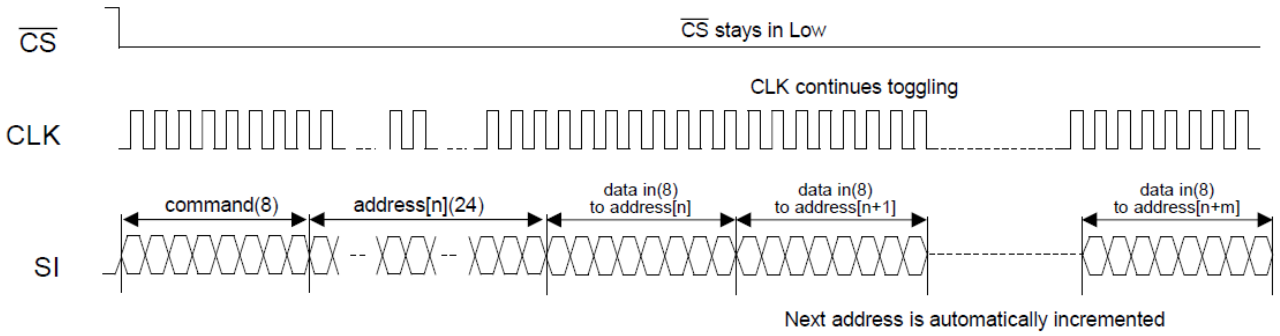


Figure 15 : Description of Continuing Write Operation (SSIP mode)



For read operation, the device offers wrap mode. Wrap bursts are confined to address aligned 16/32/64/128/256/512/1K byte boundary. The read address can start anywhere within the wrap boundary. 16/32/64/128/256/512/1K wrap configuration is set in Configuration Register 3.

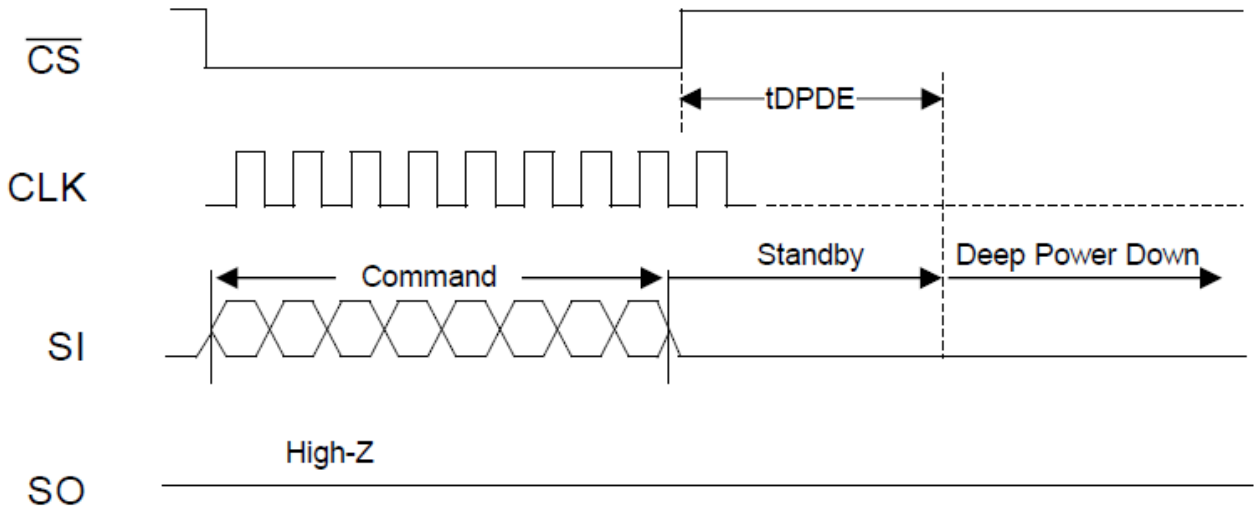
Deep Power Down Modes

The device provides Deep Power Down mode. This mode reduces current consumption from ISB to IDPD.

To enter the deep power down mode, $\overline{CS}$ is driven low, following the enter Deep Power Down (DPDE) command, $\overline{CS}$ must be driven high after the eighth bit of the command code has been latched in or the DPDE command will not be executed. After $\overline{CS}$ is driven high, it requires a delay of t_{DPDE} before the supply current is reduced to IDPD and the Deep Power Down mode is entered. The command can be issued in SPI, DSPI or QSPI modes.

reserves the right to change product or specification without notice.

Figure 16 : Entering Deep Power Down Mode (SSIP mode)

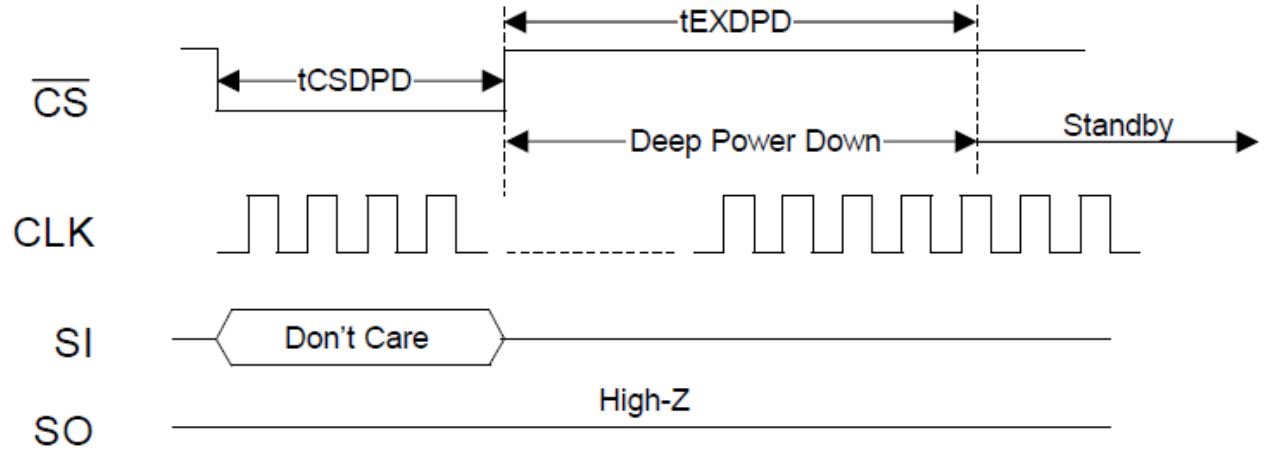


- There are two ways to exit deep power down mode:

1. Toggling $\overline{CS}$ with a $\overline{CS}$ pulse width of t_{CSDPD} while CLK and I/Os are Don't Care. During waking up from deep power down, I/Os remain to be in high-Z.

31

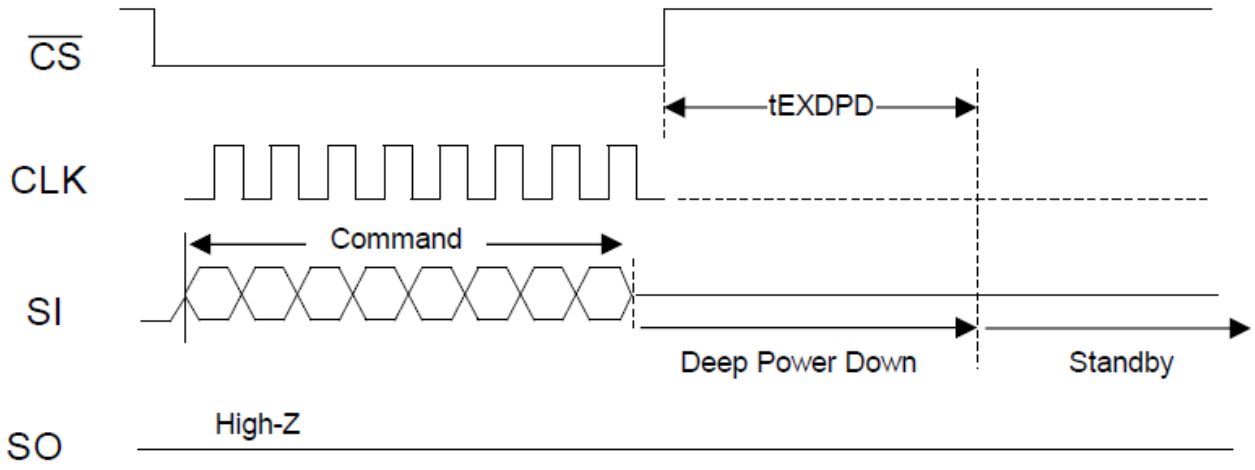
Figure 17 : Exit Deep Power Down Mode by $\overline{CS}$



2. Driving $\overline{CS}$ low follows with the Exit Deep Power Down (EXDPD, ABh) command. $\overline{CS}$ must be driven high after the eight bits of the command code has been latched in or the EXDPD command will not be executed.

reserves the right to change product or specification without notice.

Figure 18 : Exit Deep Power Down Mode by SPI Command

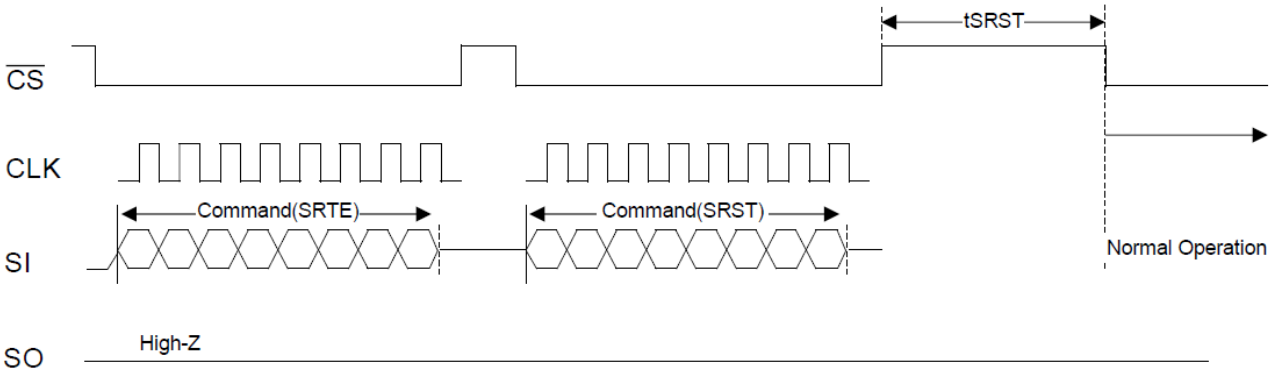


- It requires a delay of tEXDPD before the device can fully exit the deep power down mode and enter standby mode.
- Status of all non-volatile bits in registers remains unchanged when the device enters or exits the deep power down mode.
- The command can be issued in SPI, DPI, and QPI mode.

Software Reset

Software Reset (SRST) requires Software Reset Enable (SRTE) implemented in advance.

Figure 19 : Software Reset Timing



reserves the right to change product or specification without notice.

JEDEC Reset

Figure 20 : JEDEC Reset Operation Timing

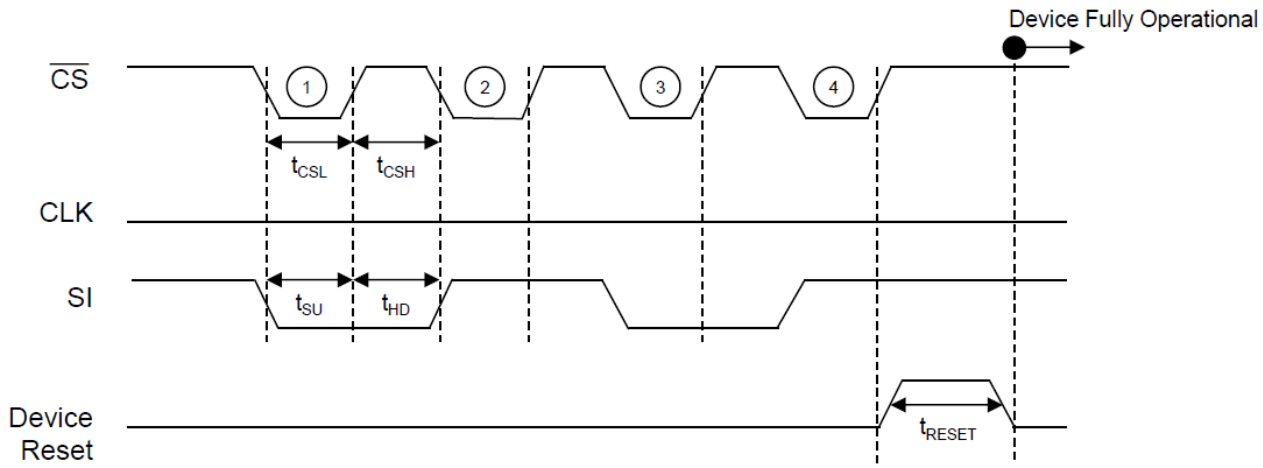


Table 28 : JEDEC Reset Operation & Timing : 1.8V Device

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Low Time	t_{CSL}	0.5	-	µs
$\overline{CS}$ High Time	t_{CSH}	0.5	-	µs
SI Setup Time (w.r.t $\overline{CS}$)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t $\overline{CS}$)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	2.0	ms

Table29 : JEDEC Reset Operation & Timing : 3.3V Device

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Low Time	t_{CSL}	0.5	-	µs
$\overline{CS}$ High Time	t_{CSH}	0.5	-	µs
SI Setup Time (w.r.t $\overline{CS}$)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t $\overline{CS}$)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	300	us

reserves the right to change product or specification without notice.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 30 : Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage on Vcc Supply Relative to VSS : 3.3V Device	-0.5	3.8	V
Voltage on Any Pin relative to VSS : 3.3V Device	-0.5	3.8	V
Voltage on Vcc Supply Relative to VSS : 1.8V Device	-0.5	2.35	V
Voltage on Any Pin relative to VSS : 1.8V Device	-0.5	2.35	V
Storage Temperature	-55	150	°C
Operating Ambient Temperature	-40	85	°C
ESD HBM (Human Body Model)	≥ |2000 V|		V
ESD CDM (Charged Device Model)	≥ |500 V|		V
Solder Reflow Process	JEDEC J-STD-020 reflow profiles Peak temperature ≤ 260°C The time above 255°C ≤ 30 seconds Reflow cycles ≤ 3 times		

Endurance, Retention and Magnetic Immunity

Table 31 : Endurance, Retention and Magnetic Immunity

Parameter	Conditions	Min.	Max.	Units
Write Endurance	-25˚C	10^{14}	-	cycles
Data Retention	85˚C	10	-	years
Magnetic Field During Write or Read	-	-	24,000	A/m

reserves the right to change product or specification without notice.

Recommended Operating Conditions

Table 32 : Recommended Operating Conditions

Parameter / Condition		Min.	Typ.	Max.	Units
Operating Temperature	Commercial	0	25	70	°C
	Industrial	-40	25	85	°C
Vcc Supply Voltage : 3.3V Device		2.7	3.3	3.6	V
Vcc Supply Voltage : 1.8V Device		1.71	1.8	1.98	V
Vss Supply Voltage		0.0	0.0	0.0	V

Pin Capacitance

Table 33 : Pin Capacitance

Parameter	Conditions	Typ.	Max.	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	-	4	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; $V_{I/O}$ = 0V	-	6	pF

AC Test Condition

Table 34 : AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to Vcc
Input rise and fall times	1ns/1V
Input and output measurement timing levels	Vcc/2
Output Load	CL = 30pF

reserves the right to change product or specification without notice.

DC Characteristics

Table 35 : DC Characteristics : 3.3V Device

Parameter	Symbol	Test Conditions	2.7V-3.6V			Units
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to Vcc (max)	-2	-	2	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to Vcc (max)	-2	-	2	µA
Read Current (1-1-1)	I_{CCR1}	SDR=54MHz, DDR=27MHz $\overline{CS}$ =0, CLK=0/Vcc, I_{OUT}=0mA	-	3	4	mA
Read Current (2-2-2)	I_{CCR2}		-	4	5	mA
Read Current (4-4-4)	I_{CCR3}		-	5	6	mA
Read Current (1-1-1)	I_{CCR4}	SDR=108MHz, DDR=54MHz $\overline{CS}$ =0, CLK=0/Vcc, I_{OUT}=0mA	-	4	5	mA
Read Current (2-2-2)	I_{CCR5}		-	6	7	mA
Read Current (4-4-4)	I_{CCR6}		-	8	10	mA
Write Current (1-1-1)	I_{CCW1}	SDR=54MHz, DDR=27MHz $\overline{CS}$ =0 ,CLK=0/Vcc, I/O=0/Vcc	-	5	6	mA
Write Current (2-2-2)	I_{CCW2}		-	8	9	mA
Write Current (4-4-4)	I_{CCW3}		-	13	16	mA
Write Current (1-1-1)	I_{CCW4}	SDR=108MHz, DDR=54MHz $\overline{CS}$ =0, CLK=0/Vcc, I/O=0/Vcc	-	8	9	mA
Write Current (2-2-2)	I_{CCW5}		-	13	17	mA
Write Current (4-4-4)	I_{CCW6}		-	25	30	mA
Standby Current	I_{SB}	CLK=0, $\overline{CS}$ = Vcc, I/O=0/Vcc	-	330	490	µA
Deep Power Down Current	I_{DPD}	CLK=0, $\overline{CS}$ = Vcc, I/O=0/Vcc	-	80	150	µA
Input High Voltage	V_{IH}	-	0.7xVcc	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level	V_{OH}	I_{OH} = -1mA	2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2mA	-	-	0.4	V

reserves the right to change product or specification without notice.

DC Characteristics

Table 36 : DC Characteristics : 1.8V Device

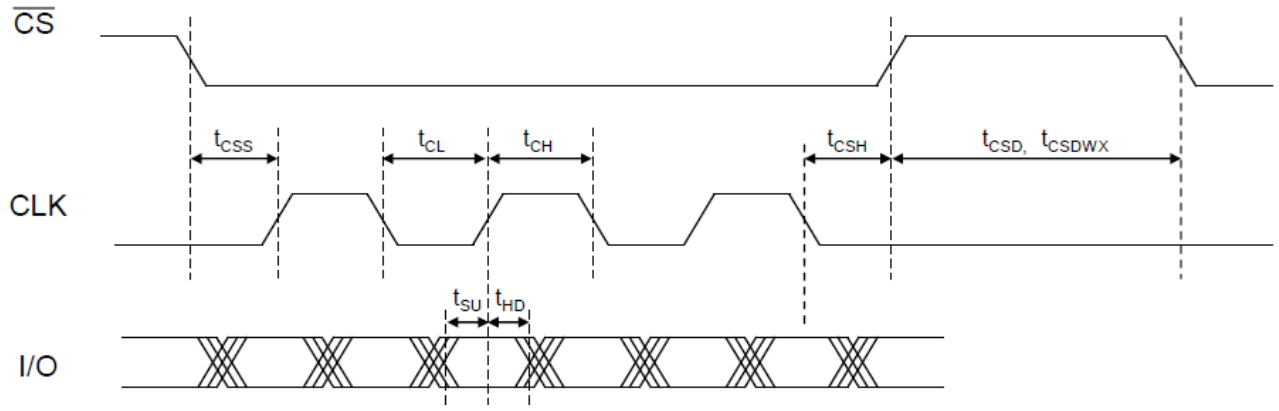
Parameter	Symbol	Test Conditions	1.71V~1.98V			Units
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to Vcc (max)	-2	-	2	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to Vcc (max)	-2	-	2	µA
Read Current (1-1-1)	I_{CCR1}	SDR=54MHz, DDR=27MHz $\overline{CS}$ =0, CLK=0/Vcc, I_{OUT}=0mA	-	2	3	mA
Read Current (2-2-2)	I_{CCR2}		-	3	4	mA
Read Current (4-4-4)	I_{CCR3}		-	4	5	mA
Read Current (1-1-1)	I_{CCR4}	SDR=108MHz, DDR=54MHz $\overline{CS}$ =0, CLK=0/Vcc, I_{OUT}=0mA	-	3	4	mA
Read Current (2-2-2)	I_{CCR5}		-	4	5	mA
Read Current (4-4-4)	I_{CCR6}		-	6	7	mA
Write Current (1-1-1)	I_{CCW1}	SDR=54MHz, DDR=27MHz $\overline{CS}$ =0 ,CLK=0/Vcc, I/O=0/Vcc	-	4	5	mA
Write Current (2-2-2)	I_{CCW2}		-	7	8	mA
Write Current (4-4-4)	I_{CCW3}		-	12	15	mA
Write Current (1-1-1)	I_{CCW4}	SDR=108MHz, DDR=54MHz $\overline{CS}$ =0, CLK=0/Vcc, I/O=0/Vcc	-	7	8	mA
Write Current (2-2-2)	I_{CCW5}		-	12	15	mA
Write Current (4-4-4)	I_{CCW6}		-	22	28	mA
Standby Current	I_{SB}	CLK=0, $\overline{CS}$ = Vcc, I/O=0/Vcc	-	280	450	µA
Deep Power Down Current	I_{DPD}	CLK=0, $\overline{CS}$ = Vcc, I/O=0/Vcc	-	25	100	µA
Input High Voltage	V_{IH}	-	0.7xVcc	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-	-0.3	-	0.3xVcc	V
Output High Voltage Level	V_{OH}	I_{OH} = -1mA	1.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2mA	-	-	0.4	V

reserves the right to change product or specification without notice.

AC Timing Characteristics

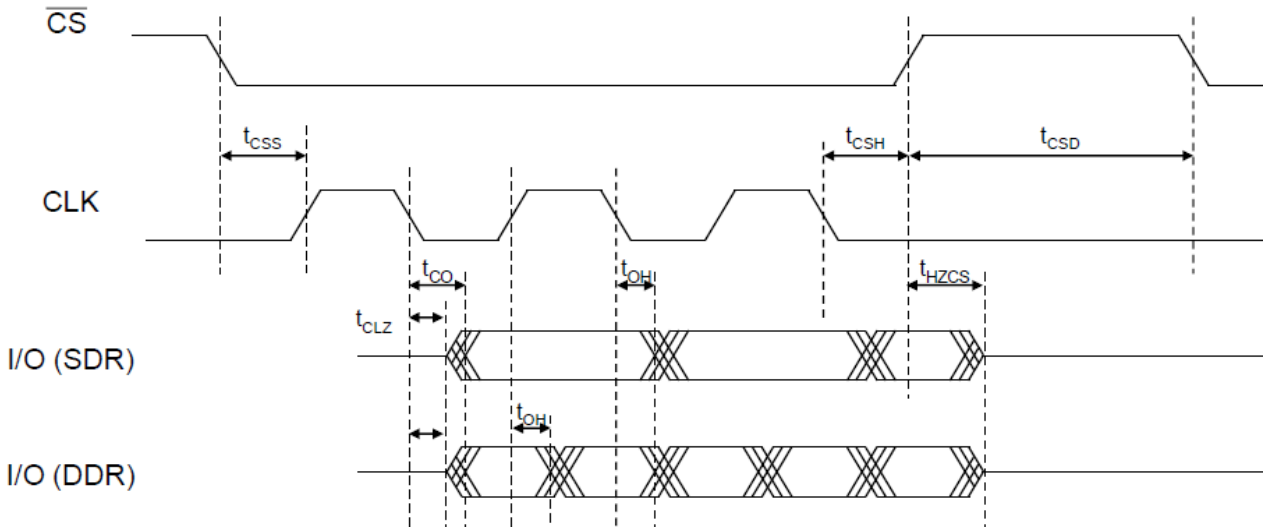
Synchronous Input Timing

Figure 21 : Synchronous Input Timing (SDR/DDR)



Synchronous Data Output Timing

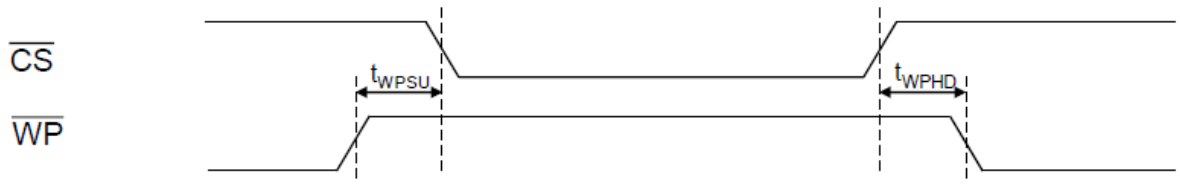
Figure 22 : Synchronous Data Output Timing (SDR/DDR)



reserves the right to change product or specification without notice.

$\overline{WP}$ Timing

Figure 23 : $\overline{WP}$ Operation Timing



$\overline{CS}$ High Time

Figure 24 : $\overline{CS}$ High Timing

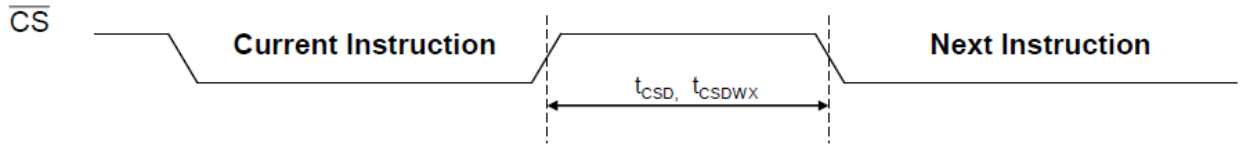


Table 37 : $\overline{CS}$ High Time after Write Instruction : SDR=108MHz/DDR=54MHz

Current Instruction : Main Array Write	Next Instruction : Main Array Read or Write	Symbol	Min.	Units
(1-1-1), (1-x-2)	(1-1-x)	t_{CSDW1}	20	ns
(1-1-1), (1-x-2)	(1-2-2)	t_{CSDW2}	130	ns
(1-x-4)	(1-1-x)	t_{CSDW3}	130	ns
(1-1-1), (1-x-2)	(1-4-4)	t_{CSDW4}	190	ns
(1-x-4)	(1-2-2), (1-4-4)	t_{CSDW5}	300	ns
(2-2-2)	(2-2-2)	t_{CSDW6}	170	ns
(4-4-4)	(4-4-4)	t_{CSDW7}	350	ns

Table 38 : $\overline{CS}$ High Time after Write Instruction : SDR=54MHz/DDR=27MHz

Current Instruction : Main Array Write	Next Instruction : Main Array Read or Write	Symbol	Min.	Units
(X-X-X)	(1-4-4)	t_{CSDW8}	70	ns
(2-2-2)	(2-2-2)	t_{CSDW9}	70	ns
(4-4-4)	(4-4-4)	t_{CSDW10}	180	ns
Others		t_{CSDW11}	20	ns

reserves the right to change product or specification without notice.

Table 39 : $\overline{CS}$ High Time after Register/Augmented 256-Byte Area Write Instruction

Current Instruction	Next Instruction	Symbol	Min.	Units
Main Array Write Instruction	Register Read/Write Augmented 256-Byte Read/Write	t_{CSDW12}	500	ns
Register Write Augmented 256-Byte Write	Any Instructions	t_{CSDW13}	1000	ns

AC Timing Parameters

Table 40 : AC Timing Parameter

Parameter	Symbol	Min.	Max.	Units
Clock Frequency – SDR	f_{CLK}	1	108	MHz
Clock Frequency – DDR	f_{CLK}	1	54	MHz
Clock Low Time	t_{CL}	0.45 * 1/ fCLK	-	ns
Clock High Time	t_{CH}	0.45 * 1/ fCLK	-	ns
$\overline{CS}$ Setup Time	t_{CSS}	5	-	ns
$\overline{CS}$ Hold Time	t_{CSH}	4	-	ns
$\overline{CS}$ High Time after Any Instruction (except Write)	t_{CSD}	20	-	ns
$\overline{CS}$ High Time after Write Instruction	t_{CSDWx}	Refer to Table 37, 38, 39		ns
Data Setup Time	t_{SU}	2	-	ns
Data Hold Time	t_{HD}	2	-	ns
CLK Low to Output Valid	t_{CO}	-	7.0	ns
CLK to Output Hold Time	t_{OH}	2.0	-	ns
CLK Low to Output Low Z (Read)	t_{CLZ}	2.0	-	ns
$\overline{CS}$ High to Output High Z	t_{HZCS}	-	6.0	ns
$\overline{WP}$ Setup Time	t_{WPSU}	20	-	ns
$\overline{WP}$ Hold Time	t_{WPHD}	20	-	ns
$\overline{CS}$ High to Power-down mode	t_{EDPD}	-	1	us
$\overline{CS}$ High to Power-down mode exit	t_{EXDPD}	-	25	us
$\overline{CS}$ Low time to exit Power-down mode	t_{CSDPD}	50	-	ns
Software Reset Time (3.3V Device)	t_{SRST}	-	0.3	ms
Software Reset Time (1.8V Device)	t_{SRST}	-	2.0	ms

reserves the right to change product or specification without notice.

Thermal Resistance

Table 41 : Thermal Resistance

Parameter	Description	8-pad WSON	8-pin SOIC	Unit
θJA	Thermal resistance (junction to ambient)	30.6	93.9	°C/W
θJC	Thermal resistance (junction to case)	19.0	31.9	

Notes:

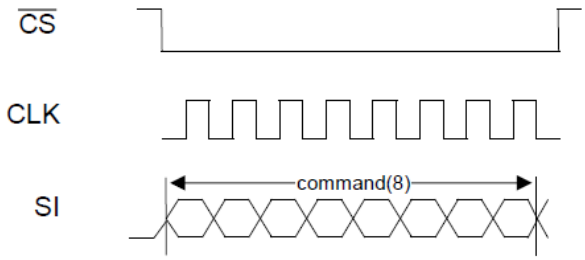
1: These parameters are guaranteed by characterization; not tested in production.

Timing Description of Instruction Sets

Single SPI – SDR (Command-Address-Data)

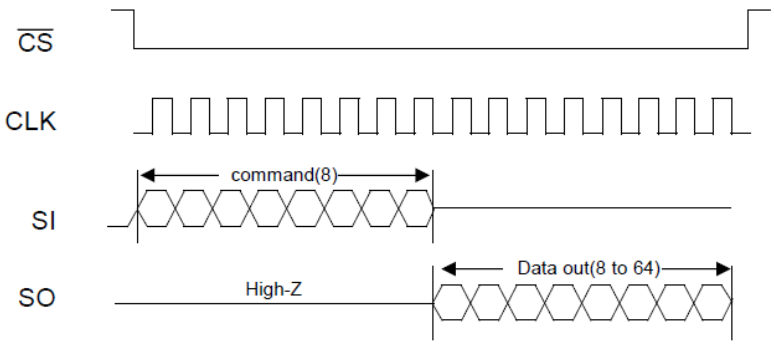
- Instruction 1-0-0 ; NOOP, WREN, WRDI, DPIE, QPIE, DPDE, DPDX, SRTE, SRST

Figure 25 : Timing Description of 1-0-0 Instruction Type



- Instruction 1-0-1 ; RDSR, RDC1, RDC2, RDC3, RDC4, RDCX, RDID, RUID, RDSN, RDAP

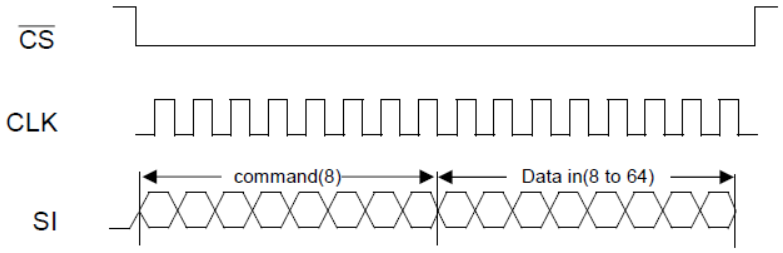
Figure 26 : Timing Description of 1-0-1 Instruction Type (Read)



reserves the right to change product or specification without notice.

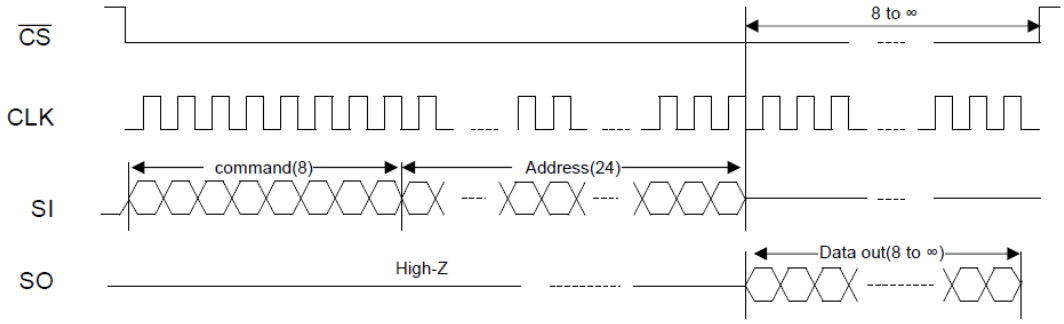
- Instruction 1-0-1 ; WRSR, WRCX, WRSN, WRAP

Figure 27 : Timing Description of 1-0-1 Instruction Type (Write)



- Instruction 1-1-1 ; READ(03h)

Figure 28 : Timing Description of 1-1-1 Instruction Type (Read without XIP)

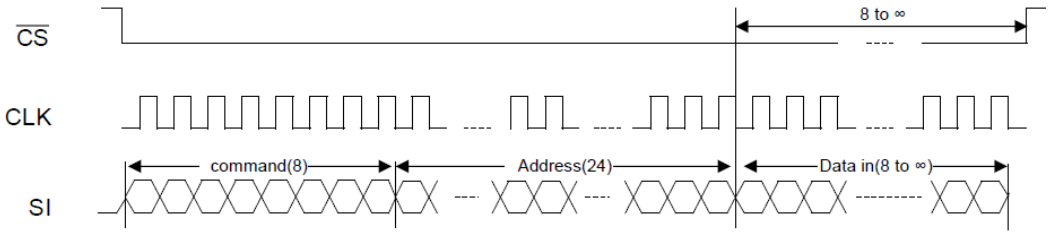


Notes:

As long as $\overline{CS}$ stays in low and CLK keeps toggling, next target address is incremented automatically, and the device keeps outputting data from memory array.

- Instruction 1-1-1 ; WRTE(02h)

Figure 29 : Timing Description of 1-1-1 Instruction Type (Write)



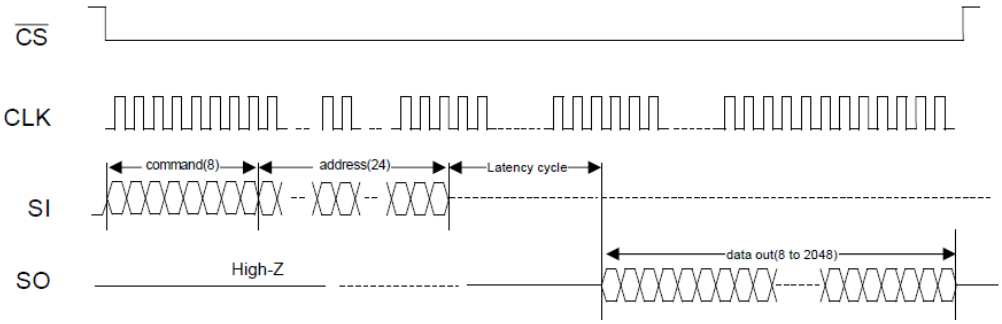
Notes:

As long as $\overline{CS}$ stays in low and CLK keeps toggling, next target address is incremented automatically, and the device keeps writing data to memory array.

reserves the right to change product or specification without notice.

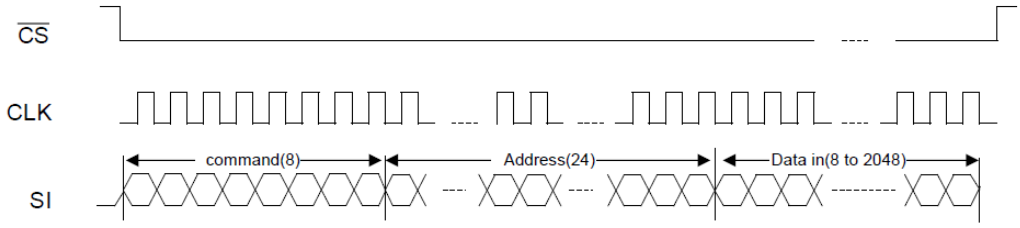
- Instruction 1-1-1 ; RDAS

Figure 30 : Timing Description of 1-1-1 Augmented 256-byte Area (Read)



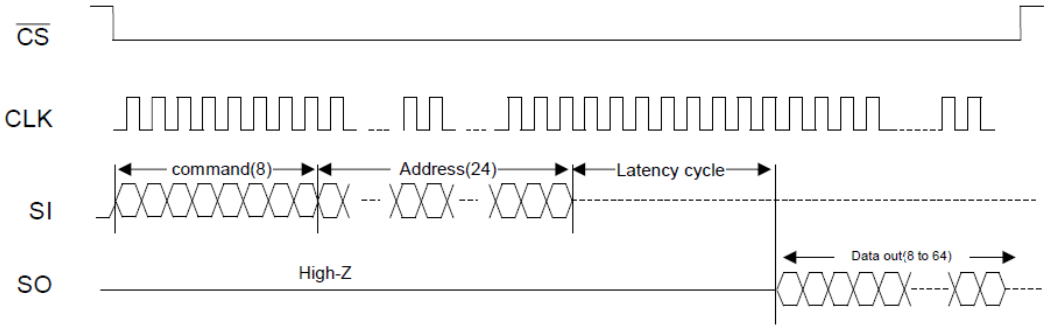
- Instruction 1-1-1 ; WRAS

Figure 31 : Timing Description of 1-1-1 Augmented 256-byte Area (Write)



- Instruction 1-1-1 ; RDAR

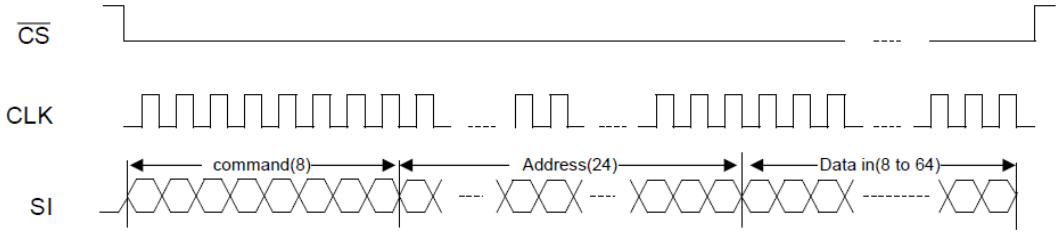
Figure 32 : Timing Description of 1-1-1 Any Register Instruction Type (Read)



reserves the right to change product or specification without notice.

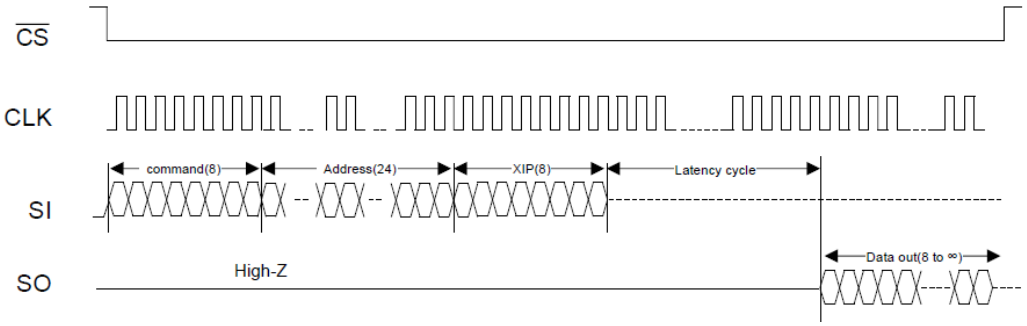
- Instruction 1-1-1 ; WRAR

Figure 33 : Timing Description of 1-1-1 Any Register Instruction Type (Write)



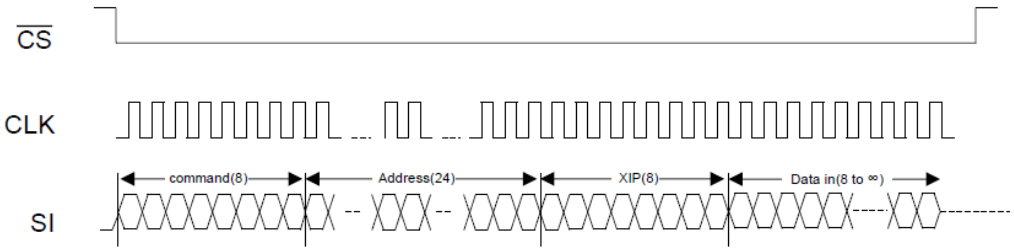
- Instruction 1-1-1 ; RDFT

Figure 34 : Timing Description of 1-1-1 Instruction Type (Read with XIP)



- Instruction 1-1-1 ; WRFT

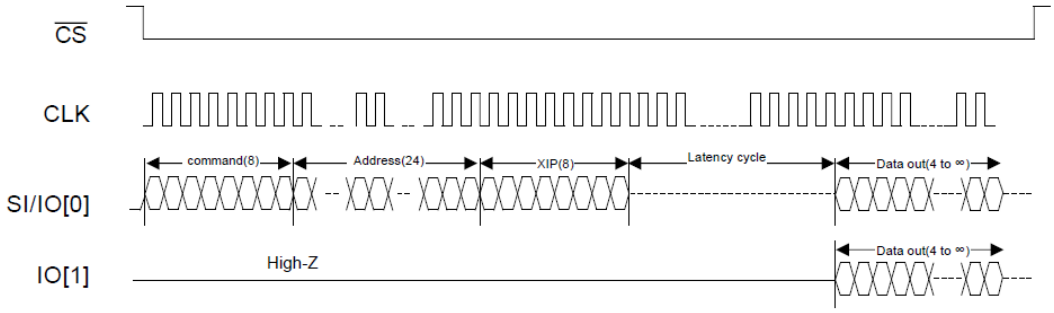
Figure 35 : Timing Description of 1-1-1 Instruction Type (Write with XIP)



reserves the right to change product or specification without notice.

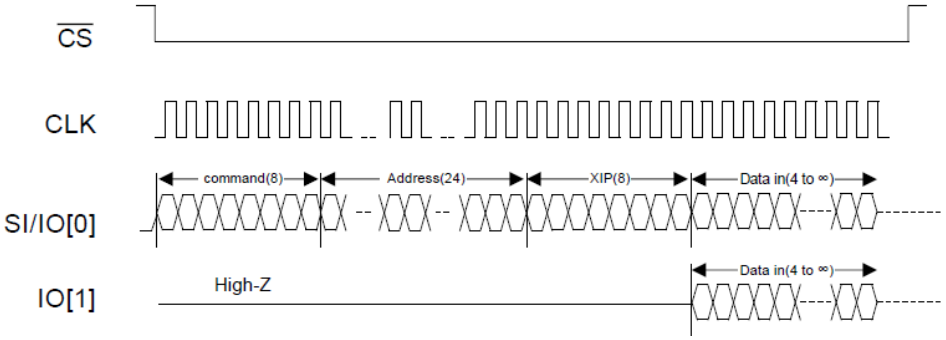
- Instruction 1-1-2 ; RDDO

Figure 36 : Timing Description of 1-1-2 Instruction Type (Read with XIP)



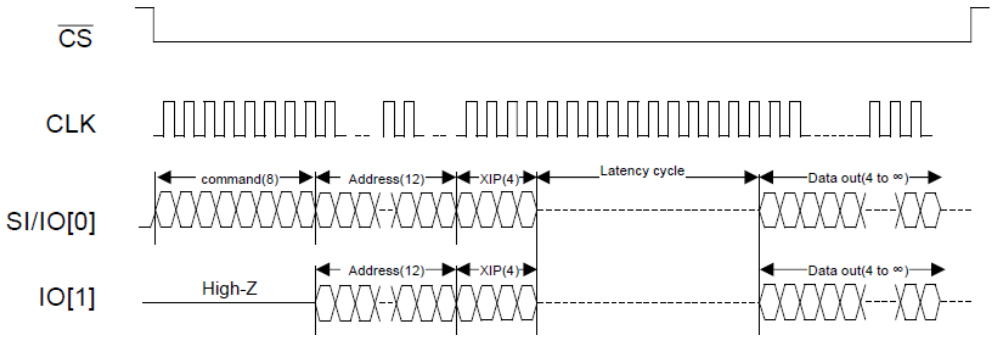
- Instruction 1-1-2 ; WDUI

Figure 37 : Timing Description of 1-1-2 Instruction Type (Write with XIP)



- Instruction 1-2-2 ; RDDI

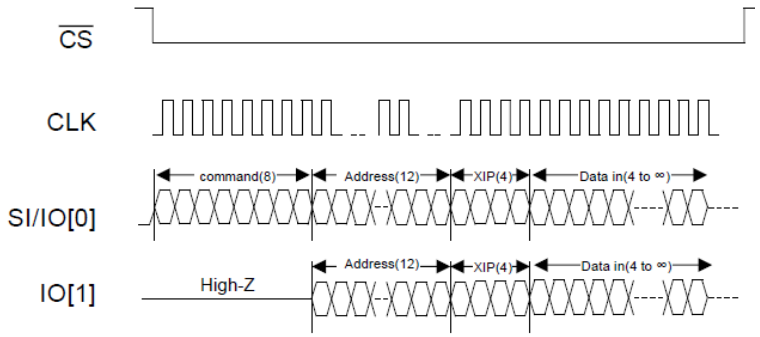
Figure 38 : Timing Description of 1-2-2 Instruction Type (Read with XIP)



reserves the right to change product or specification without notice.

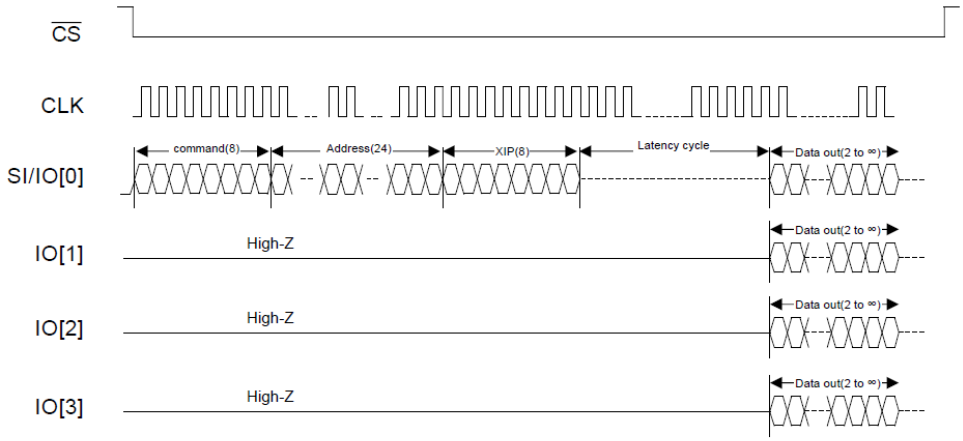
- Instruction 1-2-2 ; WDIO

Figure 39 : Timing Description of 1-2-2 Instruction Type (Write with XIP)



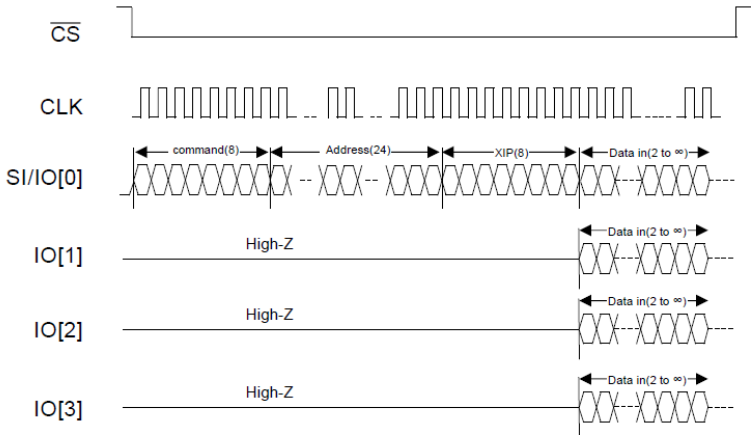
- Instruction 1-1-4 ; RDQO

Figure 40 : Timing Description of 1-1-4 Instruction Type (Read with XIP)



- Instruction 1-1-4 ; WQDI

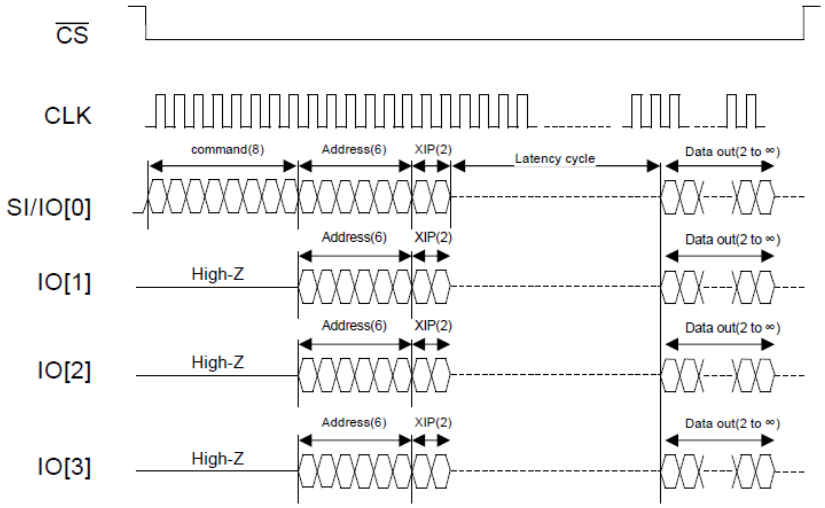
Figure 41 : Timing Description of 1-1-4 Instruction Type (Write with XIP)



reserves the right to change product or specification without notice.

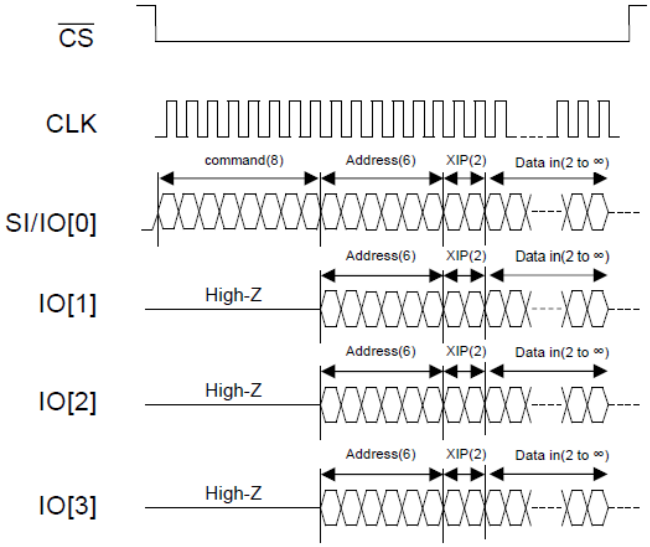
- Instruction 1-4-4 ; RDQI

Figure 42 : Timing Description of 1-4-4 Instruction Type (Read with XIP)



- Instruction 1-4-4 ; WQIO

Figure 43 : Timing Description of 1-4-4 Instruction Type (Write with XIP)

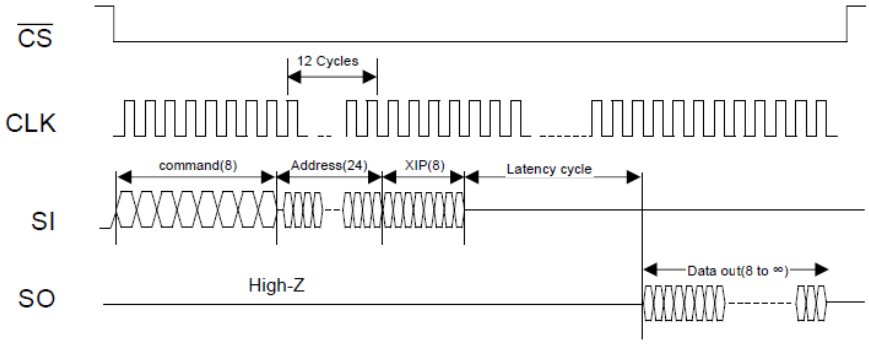


reserves the right to change product or specification without notice.

Single SPI - DDR (Command-Address-Data)

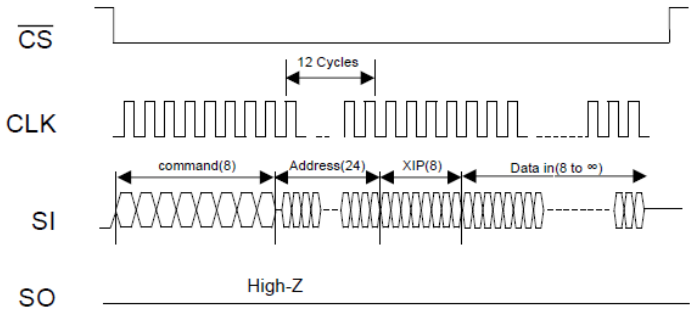
- Instruction 1-1-1 ; DRFR

Figure 44 : Timing Description of 1-1-1 DDR Instruction Type (Read with XIP)



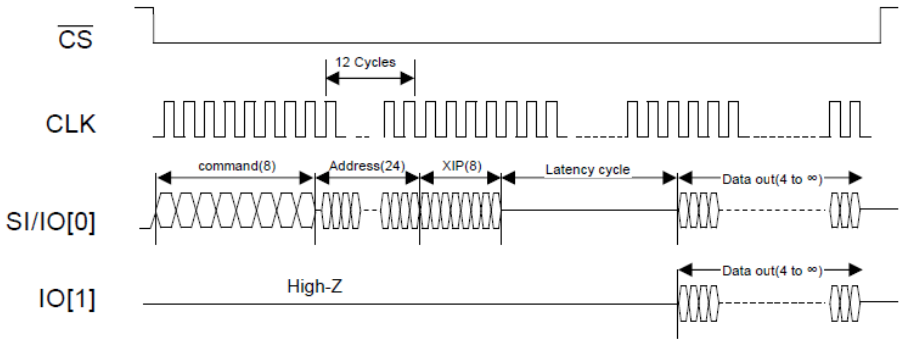
- Instruction 1-1-1 ; DRFW

Figure 45 : Timing Description of 1-1-1 DDR Instruction Type (Write with XIP)



- Instruction 1-1-2 ; DRDO

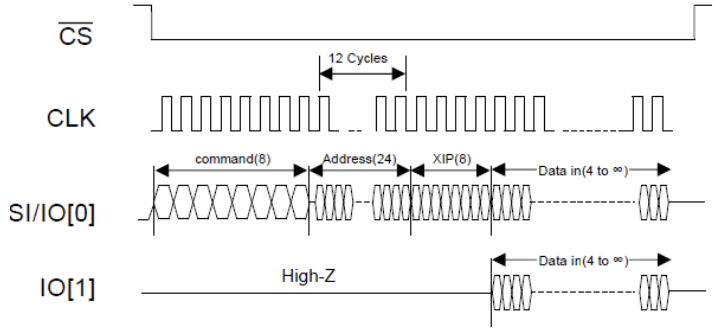
Figure 46 : Timing Description of 1-1-2 DDR Instruction Type (Read with XIP)



reserves the right to change product or specification without notice.

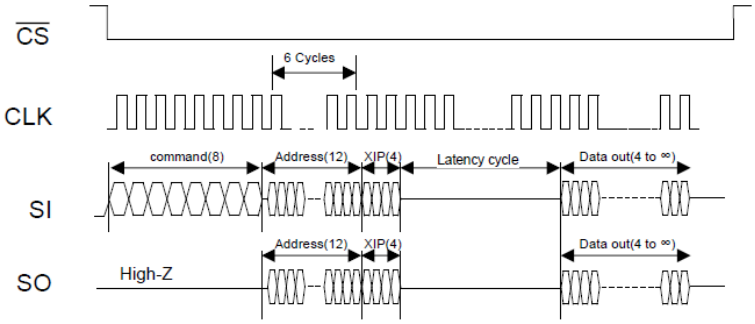
- Instruction 1-1-2 ; DWUI

Figure 47 : Timing Description of 1-1-2 DDR Instruction Type (Write with XIP)



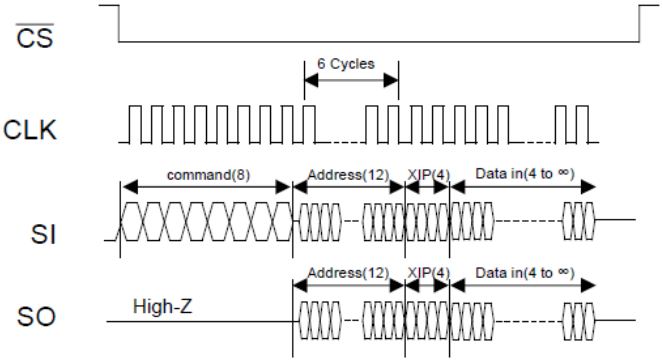
- Instruction 1-2-2 ; DRDI

Figure 48 : Timing Description of 1-2-2 DDR Instruction Type (Read with XIP)



- Instruction 1-2-2 ; DWIO

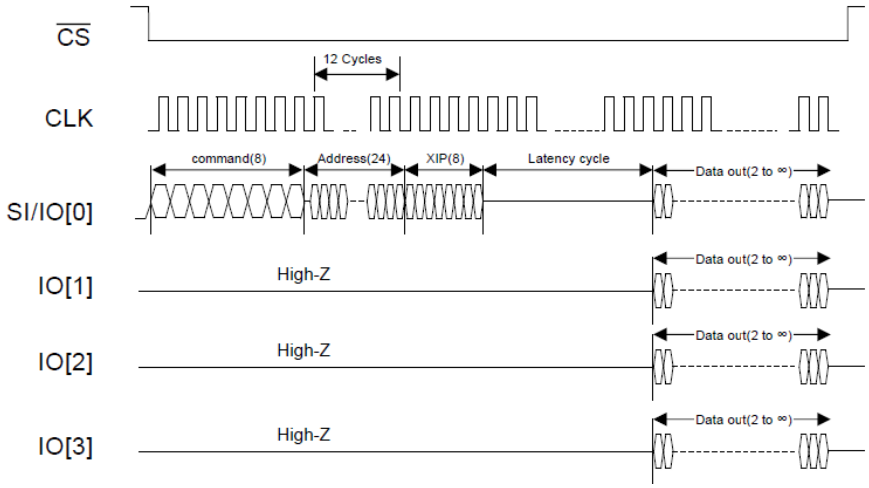
Figure 49 : Timing Description of 1-2-2 DDR Instruction Type (Write with XIP)



reserves the right to change product or specification without notice.

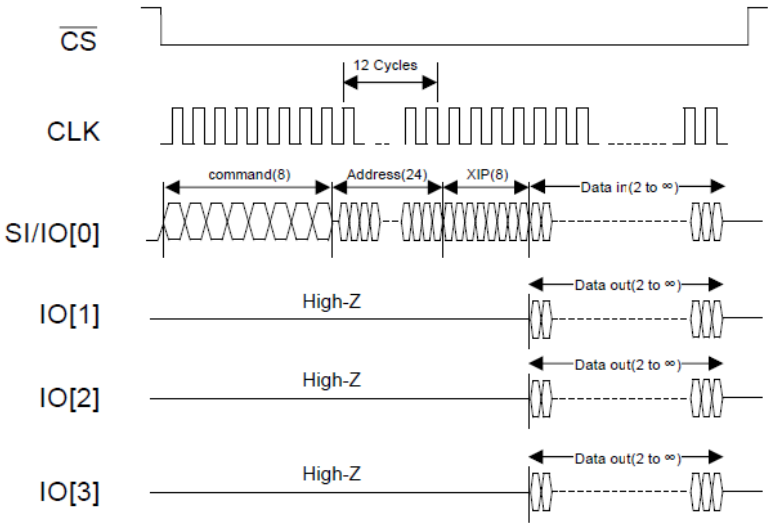
- Instruction 1-1-4 ; DRQO

Figure 50 : Timing Description of 1-1-4 DDR Instruction Type (Read with XIP)



- Instruction 1-1-4 ; DWQI

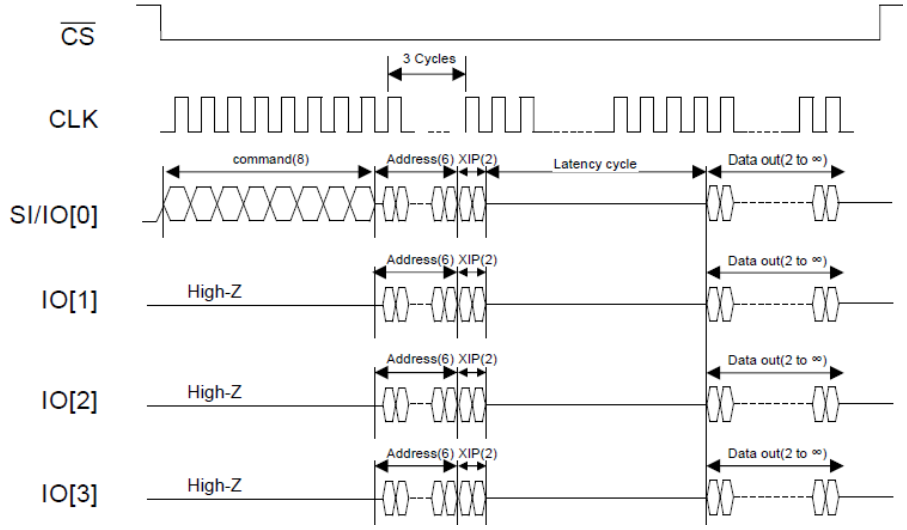
Figure 51 : Timing Description of 1-1-4 DDR Instruction Type (Write with XIP)



reserves the right to change product or specification without notice.

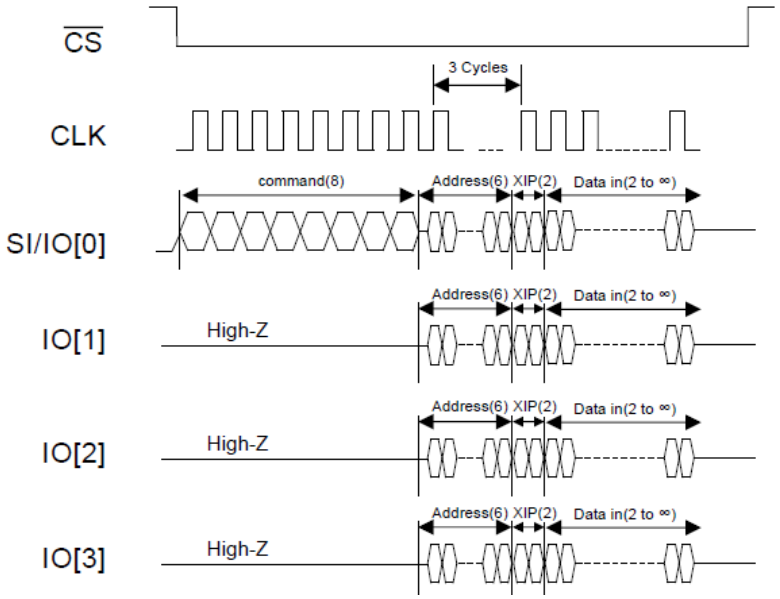
- Instruction 1-4-4 ; DRQI

Figure 52 : Timing Description of 1-4-4 DDR Instruction Type (Read with XIP)



- Instruction 1-4-4 ; DWQO

Figure 53 : Timing Description of 1-4-4 DDR Instruction Type (Write with XIP)

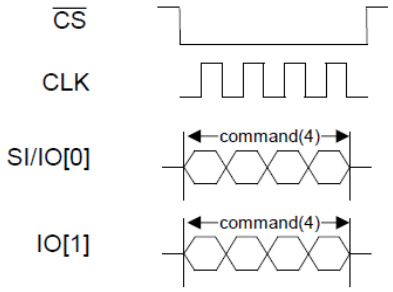


reserves the right to change product or specification without notice.

Dual SPI – SDR (Command-Address-Data)

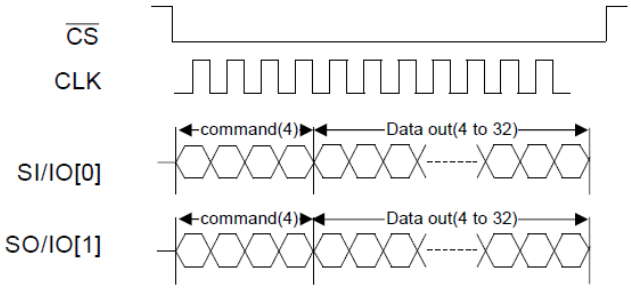
- Instruction 2-0-0 ; NOOP, WREN, WRDI, QPIE, SPIE, DPDE, DPDX, SRTE, SRST

Figure 54 : Timing Description of 2-0-0 Instruction Type



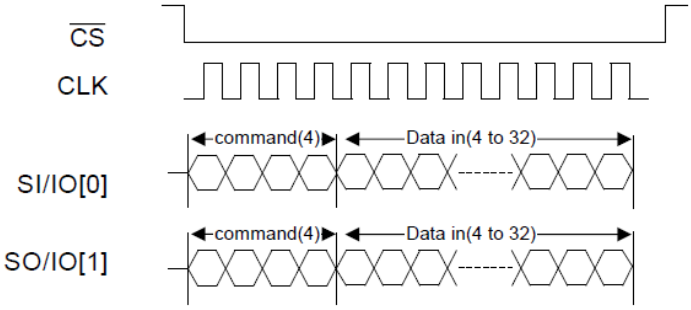
- Instruction 2-0-2 ; RDSR, RDC1, RDC2, RDC3, RDC4, RDCX, RDID, RUID, RDSN, RDAP

Figure 55 : Timing Description of 2-0-2 Instruction Type (Read)



- Instruction 2-0-2 ; WRSR, WRCX, WRSN, WRAP

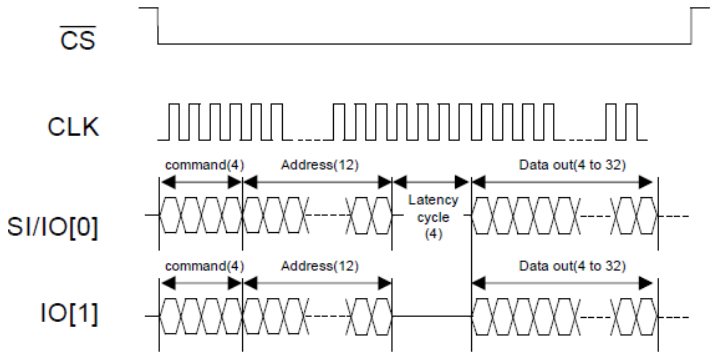
Figure 56 : Timing Description of 2-0-2 Instruction Type (Write)



reserves the right to change product or specification without notice.

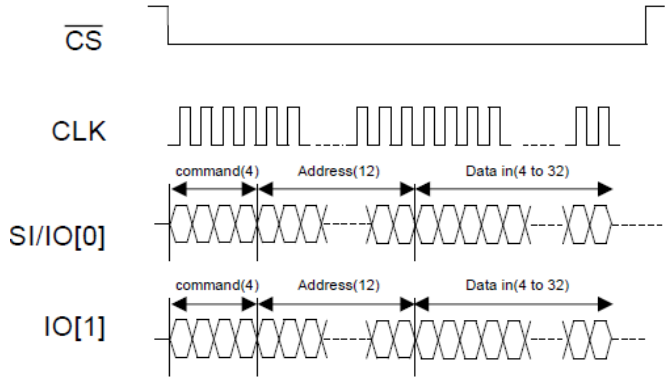
- Instruction 2-2-2 ; RDAR

Figure 57 : Timing Description of 2-2-2 Any Register Instruction Type (Read)



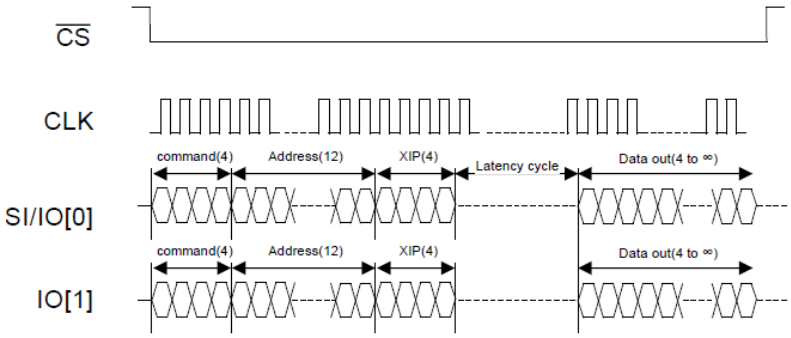
- Instruction 2-2-2 ; WRAR

Figure 58 : Timing Description of 2-2-2 Any Register Instruction Type (Write)



- Instruction 2-2-2 ; RDFT

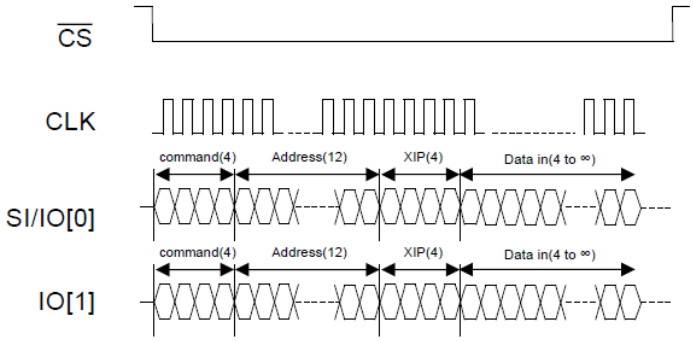
Figure 59 : Timing Description of 2-2-2 Instruction Type (Read with XIP)



reserves the right to change product or specification without notice.

- Instruction 2-2-2 ; WRFT

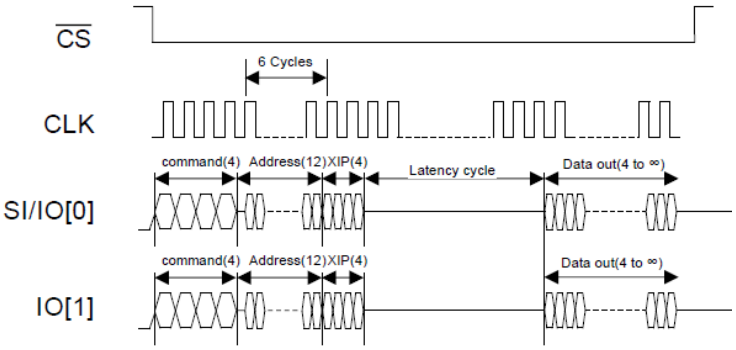
Figure 60 : Timing Description of 2-2-2 Instruction Type (Write with XIP)



Dual SPI - DDR (Command-Address-Data)

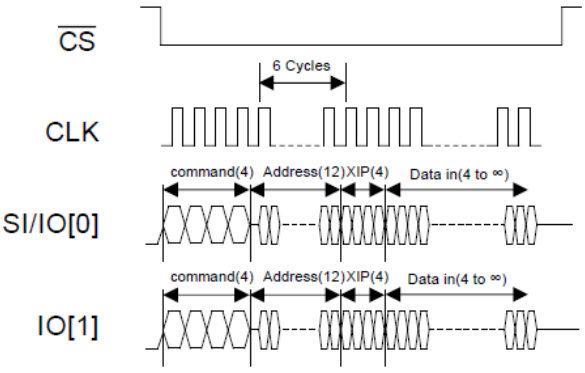
- Instruction 2-2-2 ; DRFR

Figure 61 : Timing Description of 2-2-2 DDR Instruction Type (Read with XIP)



- Instruction 2-2-2 ; DRFW

Figure 62 : Timing Description of 2-2-2 DDR Instruction Type (Write with XIP)

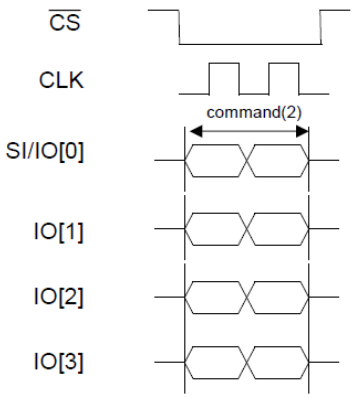


reserves the right to change product or specification without notice.

Quad SPI – SDR (Command-Address-Data)

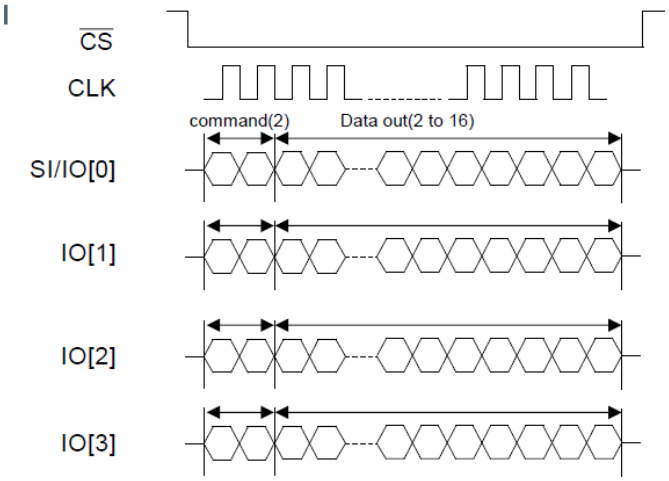
- Instruction 4-0-0 ; NOOP, WREN, WRDI, DPIE, SPIE, DPDE, DPDX, SRTE, SRST

Figure 63 : Timing Description of 4-0-0 Instruction Type



- Instruction 4-0-4 ; RDSR, RDC1, RDC2, RDC3, RDC4, RDCX, RDID, RUID, RDSN, RDAP

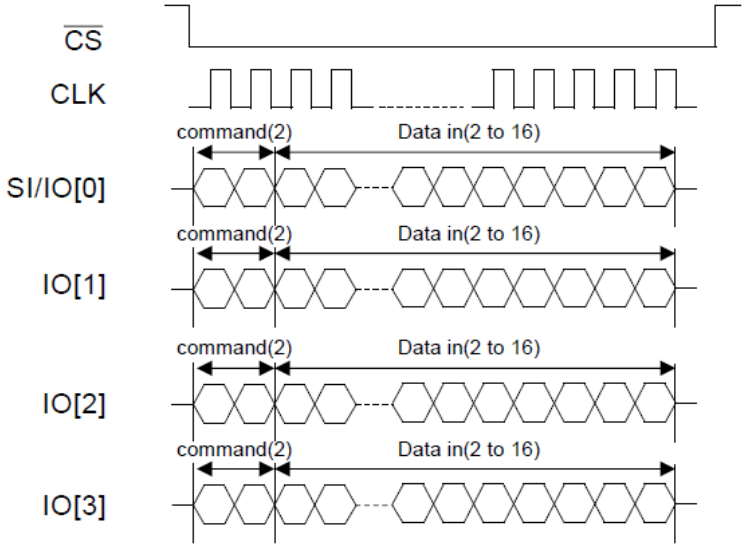
Figure 64 : Timing Description of 4-0-4 Instruction Type (Read)



reserves the right to change product or specification without notice.

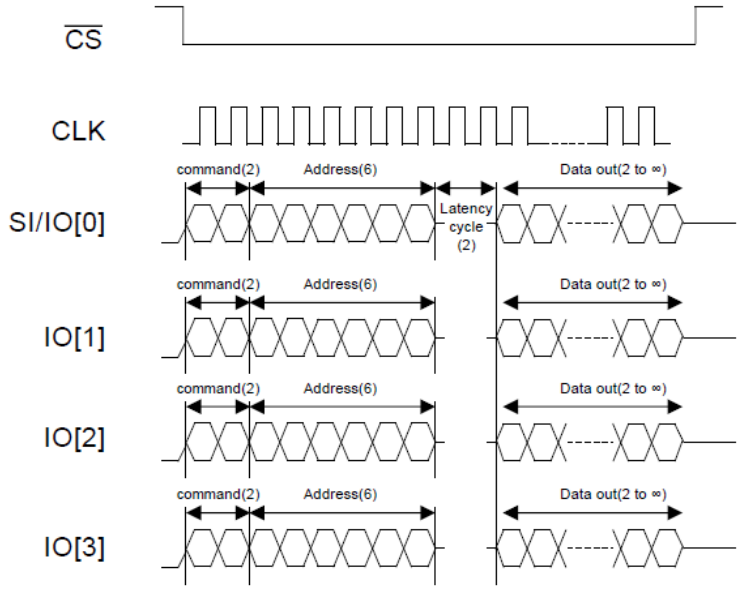
- Instruction 4-0-4 ; WRSR, WRCX, WRSN, WRAP

Figure 65 : Timing Description of 4-0-4 Instruction Type (Write)



- Instruction 4-4-4 ; RDAR

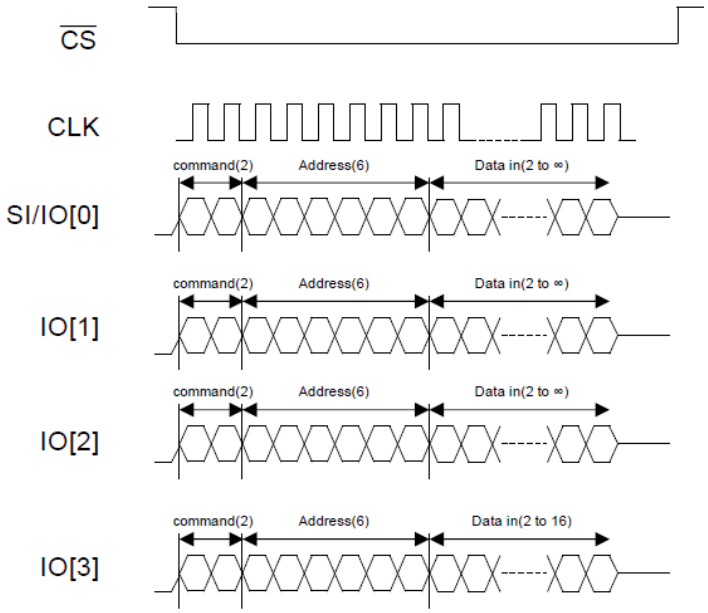
Figure 66 : Timing Description of 4-4-4 Any Register Instruction Type (Read)



reserves the right to change product or specification without notice.

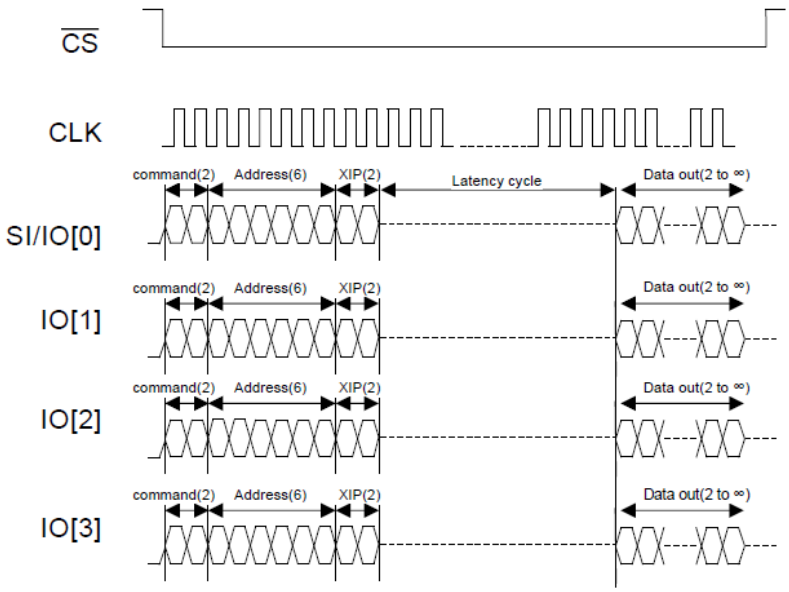
- Instruction 4-4-4 ; WRAR

Figure 67 : Timing Description of 4-4-4 Any Register Instruction Type (Write)



- Instruction 4-4-4 ; RDFT

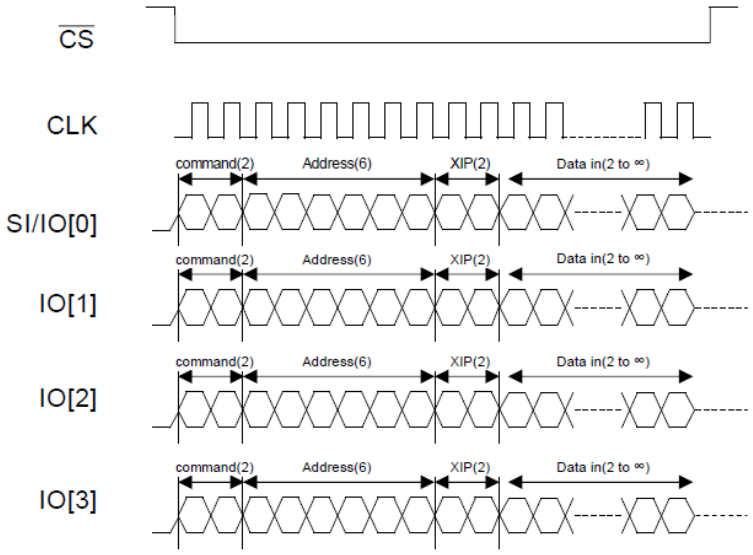
Figure 68 : Timing Description of 4-4-4 Instruction Type (Read with XIP)



reserves the right to change product or specification without notice.

- Instruction 4-4-4 ; WRFT

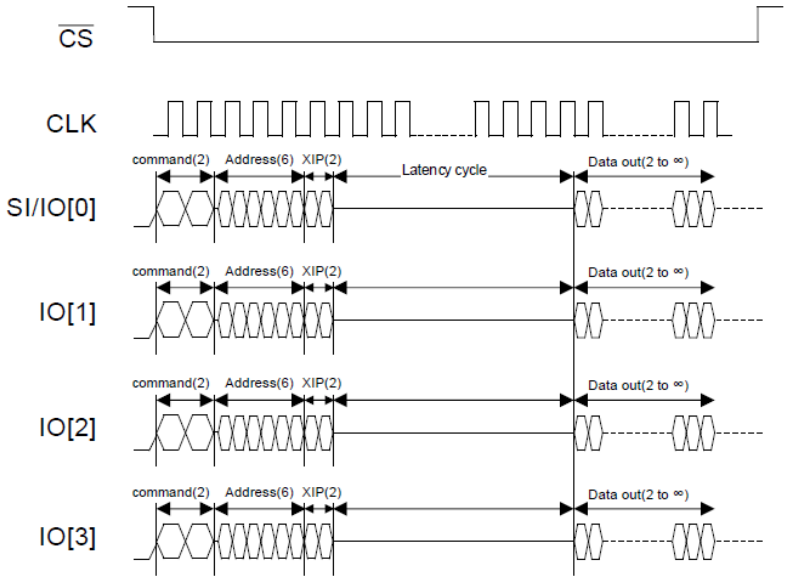
Figure 69 : Timing Description of 4-4-4 Instruction Type (Write with XIP)



Quad SPI - DDR (Command-Address-Data)

- Instruction 4-4-4 ; DRFR

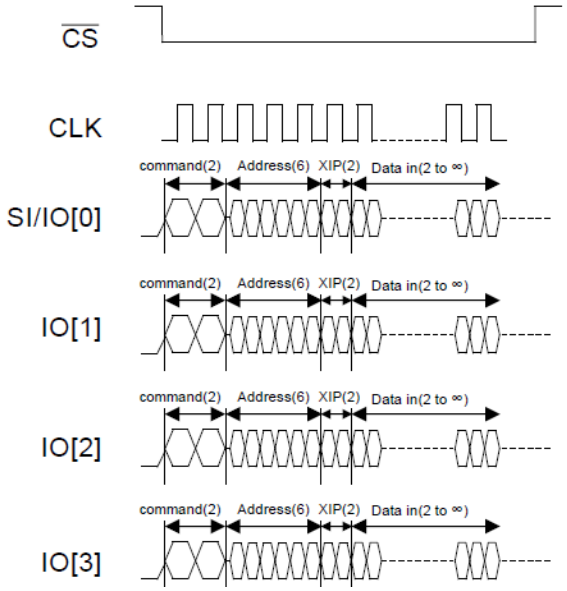
Figure 70 : Timing Description of 4-4-4 DDR Instruction Type (Read with XIP)



reserves the right to change product or specification without notice.

- Instruction 4-4-4 ; DRFW

Figure 71 : Timing Description of 4-4-4 DDR Instruction Type (Write with XIP)



Ordering Information

CS82X XX X XX X -X

Product:
82: SPI MRAM

I/O Organization:
4: x4

Density:
10: 1Mb
20: 2Mb
40: 4Mb
80: 8Mb
16: 16Mb

Voltage:
1: 1.71~1.98 V
3: 2.7V~3.6V

Speed:
9: 108 MHz

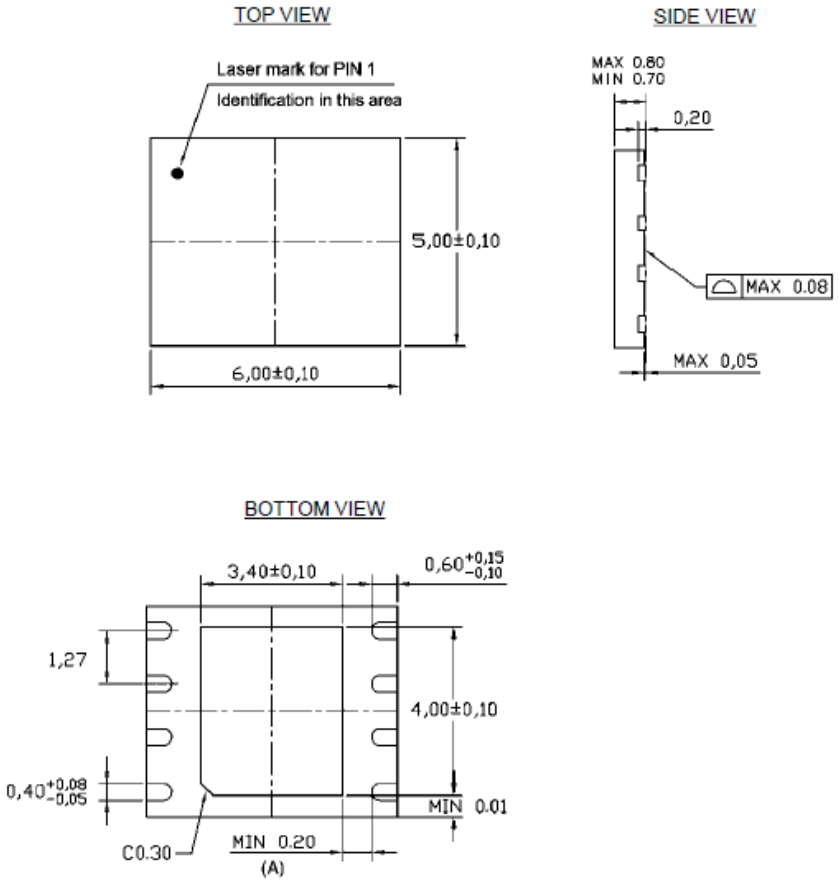
Temperature:
C: 0~70°C
I: -40~85°C

Package Type:
NP: 8L SOP-150mil
NR: 8L WSON-6x5mm

reserves the right to change product or specification without notice.

Package Dimension

8L WSON 6x5mm

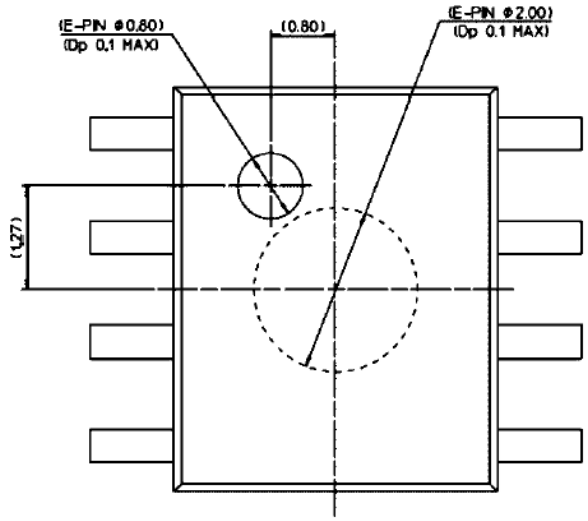


Note:

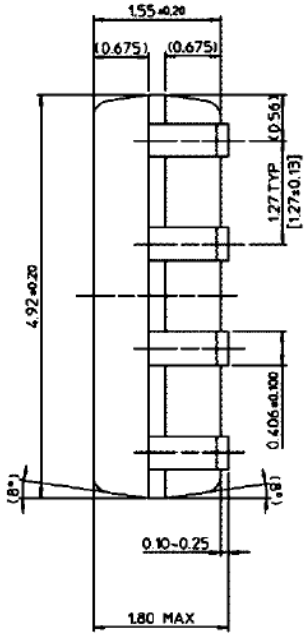
1. These dimensions do not include MOLD protrusion.
2. The exposed pad size must not violate the minimum metal separation requirement (A)
3. The PKG has exposed metal pad underneath the package, it can't contact to metal trace or pad on board.

8L SOP – 150mil

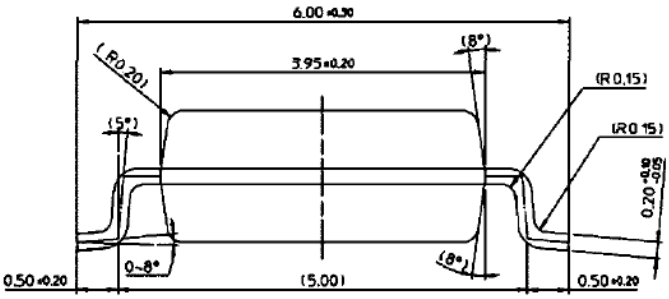
TOP VIEW



SIDE VIEW #1



SIDE VIEW #2



TITLE	8-SOP-225 PACKAGE OUTLINE	
UNIT	TOLERANCE	SCALE
mm	±0.10	N/A

reserves the right to change product or specification without notice.