Revision History

Rev. No.	History	Issue Date
1.0	New issue	Aug. 07,2023

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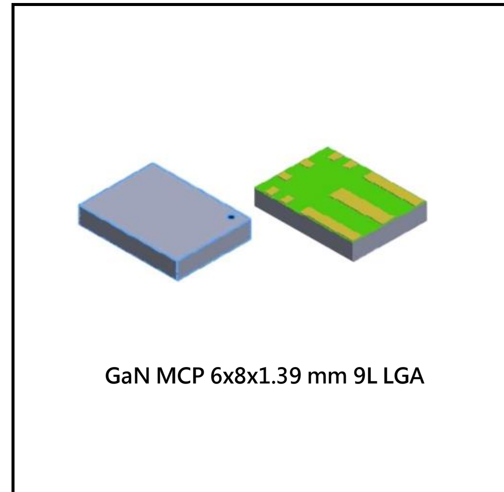
High Power GaN FET Half-Bridge Power Stage

Description

The CS9200 device is an 80V GaN power stage, driving current up to 10A, provides an integrated solution using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two 80V GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements.

The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. It is an ideal solution for applications requiring high frequency, high-efficiency operation in a small form factor.

The CS9200 device is available in a 6×8×1.39 mm 9L LGA lead-free package and can be easily mounted on PCBs.



GaN MCP 6x8x1.39 mm 9L LGA

Features

- Independent High-Side and Low-Side CMOS Logic Inputs
- Integrated 3.7mΩ GaN FETs and Driver
- High-Side input Voltage Rail Operates up to 80V
- Fast Propagation Times (30ns Typical)
- Excellent Propagation Delay Matching (2ns Typical)
- Supply Rail Under-Voltage Lockout
- Package Optimized for Easy PCB Layout, Eliminating Need for Underfill, Creepage, and Clearance Requirements

Applications

- Class D Amplifiers for Audio
- Current Fed Push-Pull converters
- Synchronous Buck converters
- Two-switch Forward converters
- High Power Density Single- and Three-Phase Motor Drive

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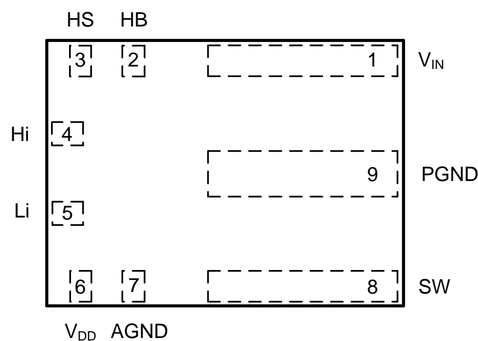
Ordering & Marking Information

CS9200 X (1)GaN FET Type (2)Part Number	(1) E: A Type GaN FET (2) N: B Type GaN FET

Pin Configuration



Top View

Pin Description

PIN NO.	SYMBOL	DESCRIPTION
1	V_{IN}	Input voltage pin.
2	HB	High–Side Bootstrap
3	HS	High–side source connection.
4	HI	High–Side Input
5	LI	Low–Side Input
6	V_{DD}	5-V positive gate drive supply.
7	AGND	Analog ground.
8	SW	Switching node. Electrically shorted to HS pin.
9	PGND	Power ground. Low-side GaN FET source.

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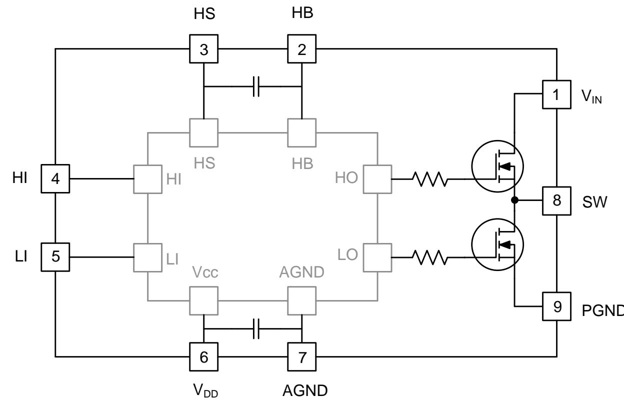
Simplified Block Diagram



Absolute Maximum Ratings (Note 1)

PARAMETER	RATINGS	UNIT
V_{IN} to PGND	0 ~ +80	V
HB to AGND	-0.3 ~ +87	V
HS to AGND	−5 ~ +80	V
V_{DD} to AGND	-0.3 ~ +7	V
HB to HS	-0.3 ~ +7	V
HB to V_{DD}	0 ~ +80	V
SW to PGND	−5 ~ +80	V
LI or HI Input	-0.3 ~ +7	V
Junction Temperature	125	°C
Storage Temperature Range	−40 ~ +150	°C

Recommended Operation Conditions (Note 2)

PARAMETER	RATINGS	UNIT
V_{IN}	0 ~ +80	
V_{DD}	+4.5 ~ +5.5	V
LI or HI Input	0 ~ +5.5	V
HS	−5 ~ 80	V
HB	V_{HS} +4 ~ V_{HS} +5.5	V
HS Slew Rate	<50	V/ns
Junction Temperature	−40 ~ +125	°C

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device.
These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: Design properly at all application environment, the device is not guaranteed to function outside its operating conditions.

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Electrical Characteristics

Typical values represent the most likely parametric norm at T_A=25°C, and are provided for reference purposes only.
Unless otherwise specified, V_{DD}=V_{HB}=5V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
V_{DD} Quiescent Current	I_{DD}	LI=HI=0V, V_{DD}=V_{HB}=5V		0.08		mA
V_{DD} Operating Current	I_{DDO}	f=500kHz		4.5		mA
Total HB Quiescent Current	I_{HB}	LI=HI=0V		0.09		mA
Total HB Operating Current	I_{HBO}	f=500kHz		4.5		mA
INPUT						
Input Voltage Threshold	V_{IR}	Rising Edge	1.85	2	2.15	V
Input Voltage Threshold	V_{IF}	Falling Edge	1.55	1.7	1.85	V
Input Voltage Hysteresis	V_{IHYS}			300		mV
Input Pulldown Resistance	R_I			200		kΩ
UNDER VOLTAGE PROTECTION						
V_{DD} rising threshold	V_{DDR}		3.2	3.8	4.5	V
V_{DD} threshold hysteresis	V_{DDH}			0.25		V
HB rising threshold	V_{HBR}		2.4	3.1	3.8	V
HB threshold hysteresis	V_{HBH}			0.25		V
POWER STAGE						
High-side GaN FET on-resistance	$R_{DS(ON)HS}$	LI=0V, HI=V_{DD}=5V, HB-HS=5V, V_{IN}-SW=5A, T_J = 25℃		3.7	4.5	mΩ
Low-side GaN FET on-resistance	$R_{DS(ON)LS}$	LI=V_{DD}=5V, HI=0V, HB-HS=5V, SW-PGND=5A, T_J = 25℃		3.7	4.5	mΩ
SW to V_{IN} Forward Voltage	V_{SD}	I_{SD}=500mA, V_{IN} floating, V_{DD}=5V, HI=LI=0V		1.5		V
Leakage from V_{IN} to SW, the high-side and low-side GaN FET are off	$I_{L-VIN-SW}$	V_{IN}=80V, HI=LI=0V, V_{DD}=5V, T_J=25℃		80	350	µA
Leakage from SW to GND, the high-side and low-side GaN FET are off	$I_{L-SW-GND}$	SW=80V, HI=LI=0V, V_{DD}=5V, T_J=25℃		80	350	µA

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Electrical Characteristics (continued)

Typical values represent the most likely parametric norm at T_A=25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD}=V_{HB}=5V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
BOOTSTRAP DIODE AND CLAMP						
Low Current forward voltage	V_{DL}	I_{VDD-HB}=100μA		0.4		V
High Current forward voltage	V_{DH}	I_{VDD-HB}=50mA		0.9		V
Dynamic resistance	R_D	I_{VDD-HB}=50mA		1.85	3.6	Ω
HB-HS clamp regulation voltage	V_{CLAMP}		4.5	5	5.5	V

■ Switching Characteristics (over operating free-air temperature range)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay: HI Rising	t_{HIPLH}	LI=0V, V_{DD}=5V, HB-HS=5V, V_{IN}=30V		30	60	ns
Propagation delay: HI Falling	t_{HIPHL}	LI=0V, V_{DD}=5V, HB-HS=5V, V_{IN}=30V		30	60	ns
Propagation delay: LI Rising	t_{LPLH}	HI=0V, V_{DD}=5V, HB-HS=5V, V_{IN}=30V		30	60	ns
Propagation delay: LI Falling	t_{LPHL}	HI=0V, V_{DD}=5V, HB-HS=5V, V_{IN}=30V		30	60	ns
Delay matching: LI high & HI low	t_{MON}			2	8	ns
Delay matching: LI low & HI high	t_{MOFF}			2	8	ns
Minimum input pulse width that changes the output	t_{PW}			10		ns

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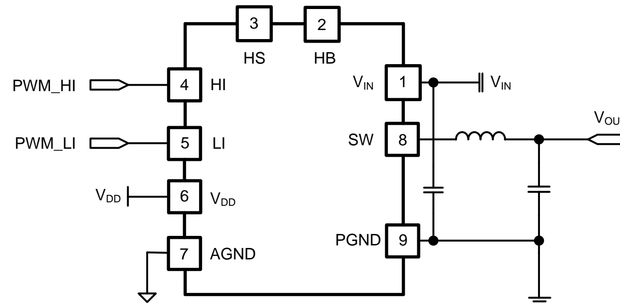
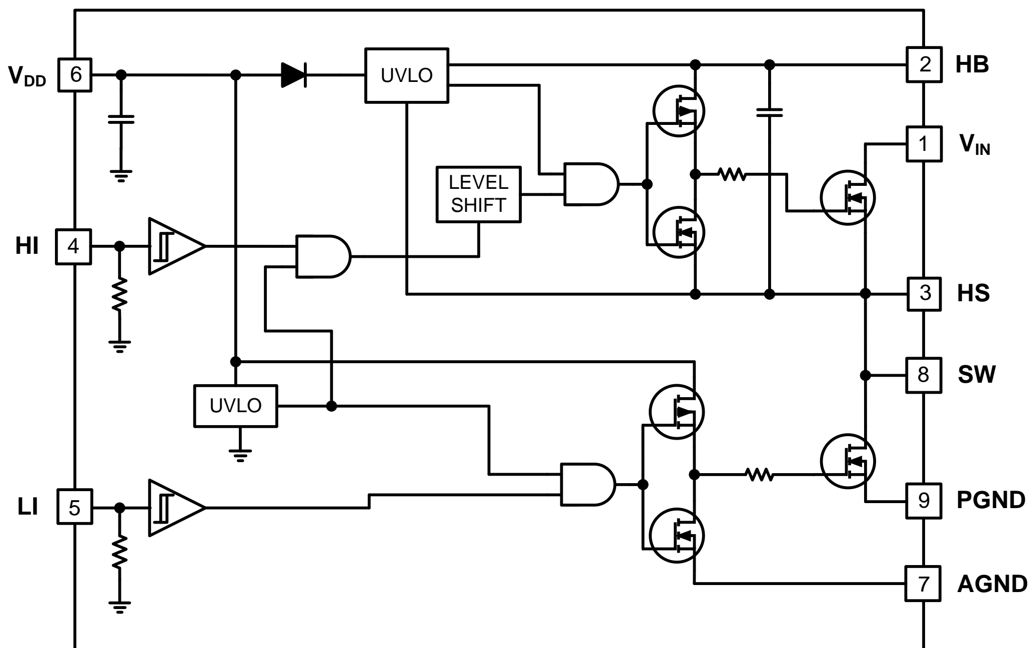
■ Typical Application Circuit



■ Functional Block Diagram



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Detailed Operating Description

The CS9200 is half-bridge, GaN power stage with highly integrated high-side and low-side gate drivers, which includes built-in UVLO protection circuitry and an overvoltage clamp circuitry. The device integrates two, 3.7mΩ GaN FETs in a half-bridge configuration. The device can be used in many isolated and non-isolated topologies allowing very simple integration. The LGA package is designed to minimize the loop inductance while keeping the PCB design simple.

The built-in bootstrap circuit with clamp prevents the high-side gate drive from exceeding the GaN FETs maximum gate-to-source voltage without any additional external circuitry. The built-in driver has an undervoltage lockout (UVLO) on the V_{DD} and bootstrap (HB-HS) rails. When the voltage is below the UVLO threshold voltage, the device ignores both the HI and LI signals to prevent the GaN FETs from being partially turned on.

PWM Inputs

The CS9200's inputs pins are independently controlled. This inputs to be directly connected to the outputs of an analog PWM controller with to 5V power supply. Allow flexibility to optimize deadtime according to design needs, the CS9200 does not implement an overlap protection functionality. If both HI and LI are asserted, both the high-side and low-side GaN FETs are turned on. Careful consideration must be applied to the control inputs in order to avoid a shoot-through condition.

High-Side Driver

The high-side driver is designed to “float” meaning that its reference (ground) floats with the SW pin of the CS9200 which is normally tied to the source of an N channel GaN FET. The bias voltage to the high-side driver is supplied to the HB pin through a bootstrap switch (diode), so that a internal capacitor(HB-HS), can be charged up each time the low side GaN device is turned on. As the high-side GaN FET turns on, SW rises to V_{IN}, forcing the HB pin voltage to $V_{IN}+V_{DD}$ that provides a voltage to hold the high-side GaN FET on.

The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5V(typ). This clamp prevents the gate voltage from exceeding the maximum gate-source voltage rating of the enhancement-mode GaN FETs.

Low-Side Driver

The low-side driver is designed to drive a ground referenced GaN FET. The bias to the low-side driver is internally connected to V_{DD} supply and GND.

Start-up and UVLO

The CS9200 has an Under-voltage Lockout (UVLO) on both the V_{DD} and bootstrap supplies. When the V_{DD} voltage is below the threshold voltage of 3.8V, both the HI and LI inputs are ignored, to prevent the FETs from being partially turned on. Also if there is sufficient V_{DD} voltage, the driver actively pulls the high-side and low-side gate driver output low. The UVLO threshold hysteresis of 200 mV prevents chattering and unwanted turnon due to voltage spikes.

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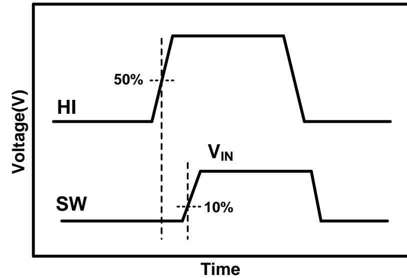
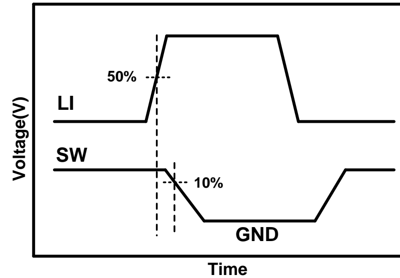
Propagation Delay Measurement

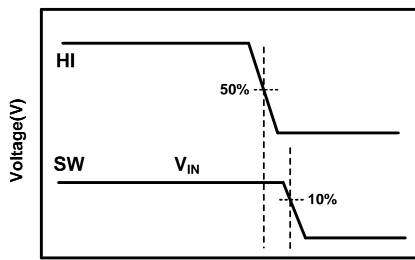
Below figure shows the definitions of the turn-on and turn-off propagation delay times.



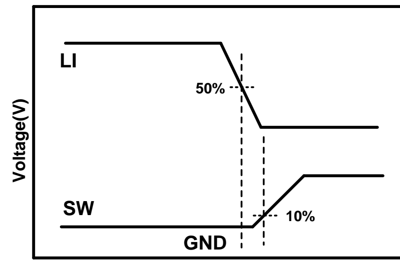
High-side Gate Driver Turn on



Low-side Gate Driver Turn on

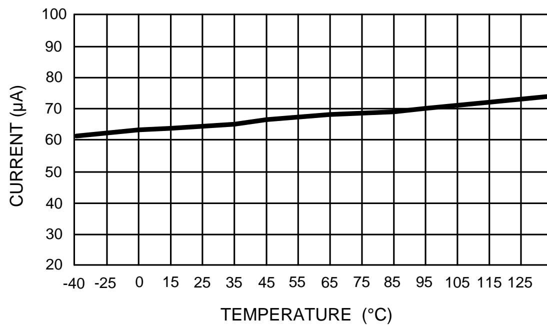


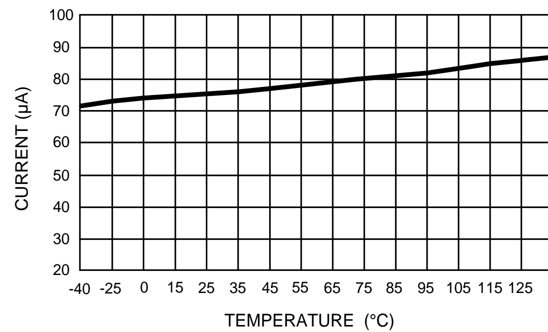
High-side Gate Driver Turn off

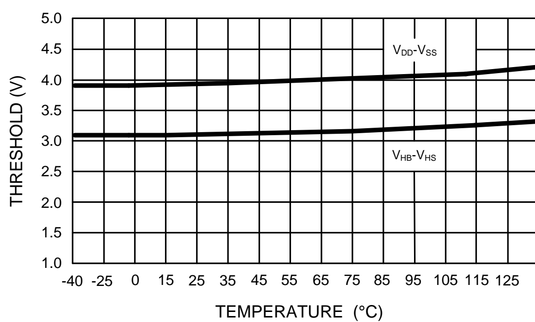


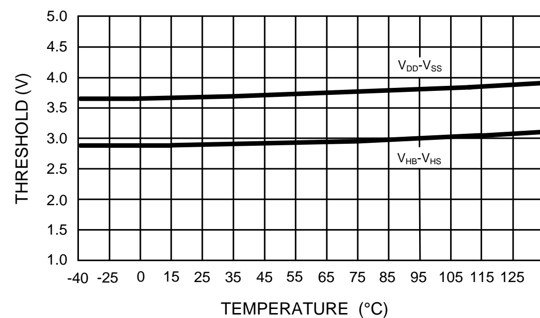
Low-side Gate Driver Turn off

Typical Characteristics









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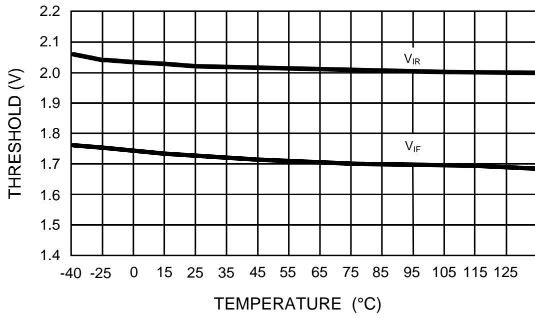
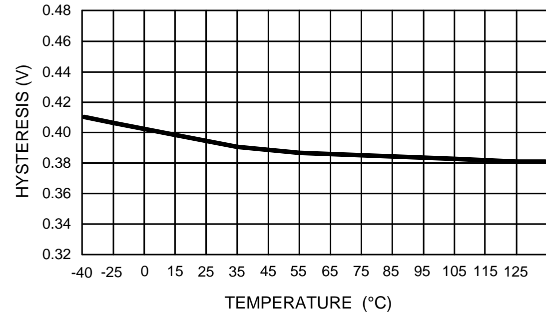
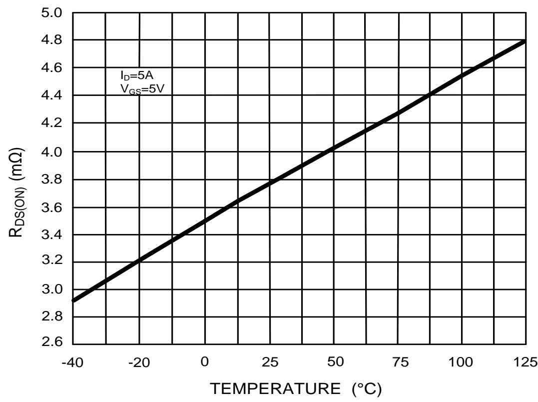
■ Typical Characteristics (continued)







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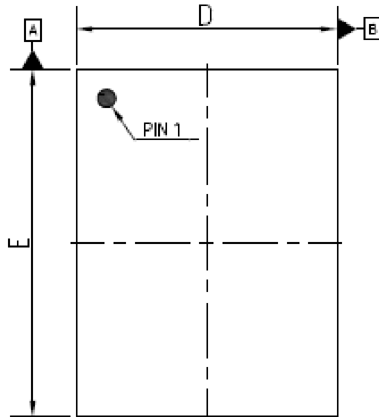
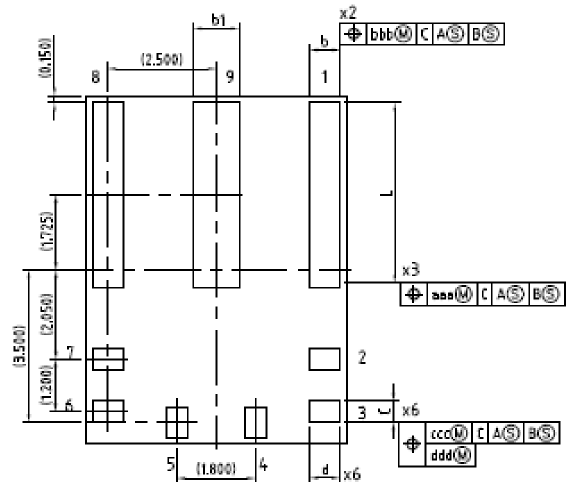
Package Dimension

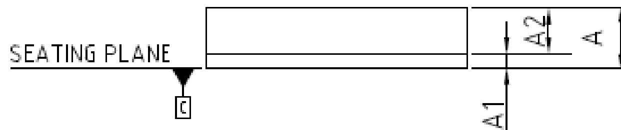
9L LGA package outline 6 x 8 x 1.39 mm body size



Top View



Bottom View



Side View

Symbol	Dimension in mm		
	Min	Norm	Max
A	1.33	1.39	1.44
A1	0.30	0.34	0.38
A2	1.03	1.05	1.06
D	5.90	6.00	6.10
E	7.90	8.00	8.10
b	0.65	0.70	0.75
b1	1.00	1.05	1.10
L	4.20	4.25	4.30
c	0.45	0.50	0.55
d	0.65	0.70	0.75
aaa	0.05		
bbb	0.05		
ccc	0.10		
ddd	0.08		

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