Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20230012	Jul.14 -2023	New issue	Hank Lin

CS81xx

1Mb ~ 16Mb PPI MRAM

General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM). Data is always non-volatile, and the device can replace FRAM, low-power SRAM or nvSRAM with same functionality and help to simplify system design. Due to the non-volatility and virtually unlimited endurance characteristics of STT-MRAM, it is suited for code storage, data logging, backup memory and working memory in industrial designs.

It is offered in density ranging from 1Mbit to 16Mbit. It is a fully random-access memory with parallel asynchronous interface. x16 or x8 I/O mode are supported. And x16 I/O mode allows that lower- and upper-byte access by data byte control ($\overline{LB}$, $\overline{UB}$).

It supports the asynchronous page mode function to enhance the read and write performance. The page size of x16 I/O mode and x8 I/O mode is 4 words and 8 words. CS81xx is packaged in industrial standard 44TSOP2, 54TSOP2 and 48TFBGA. The CS81xx is packaged in industrial standard 44TSOP2 and 48FBGA. These packages are compatible with similar low-power volatile and non-volatile products. The device is offered with industrial (-40°C to 85°C) operating temperature range.

Product Performance

Operation		Symbol	Typical Values		Unit
			1.8V	3.3V	
Interpage Read Cycle Time		t_{RC}	70(Min.)	70(Min.)	ns
Intrapage Read Cycle Time		t_{PRC}	15(Min.)	15(Min.)	ns
Interpage Write Cycle Time		t_{WC}	320(Min.)	320(Min.)	ns
Intrapage Write Cycle Time		t_{PWC}	15(Min.)	15(Min.)	ns
Standby Current	16Mb	I_{SB}	300	350	uA
	1Mb~8Mb		185	235	
Interpage Read Current		I_{CCR}	9	12	mA
Intrapage Read Current		I_{CCRP}	9	12	mA
Interpage Write Current		I_{CCW}	14	15	mA
Intrapage Write Current		I_{CCWP}	14	15	mA

Features

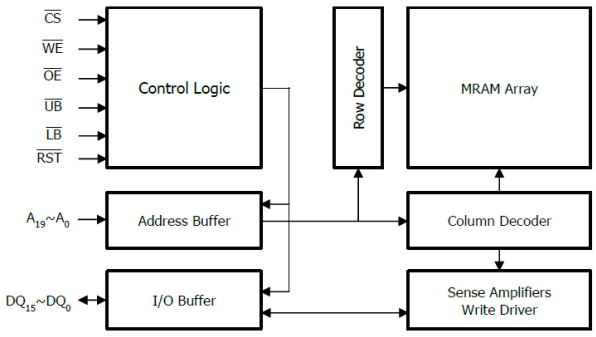
- Interface
  - Parallel Asynchronous and Page Mode Interface
- Page Mode Read Access
  - Interpage read access: 70ns
  - Intrapage read access: 15ns
- Page Mode Write Access
  - Interpage write access: 320ns
  - Intrapage write access: 15ns
- Page Size
  - X16 I/O Mode: 4-word page size
  - X8 I/O Mode: 8-word page size
- Low Power Consumption

Items	1.8V		3.3V	
	X16	X8	X16	X8
Read current:	9mA		12mA	
Write current	14mA		15mA	
Standby current:	300uA	185uA	350uA	235uA

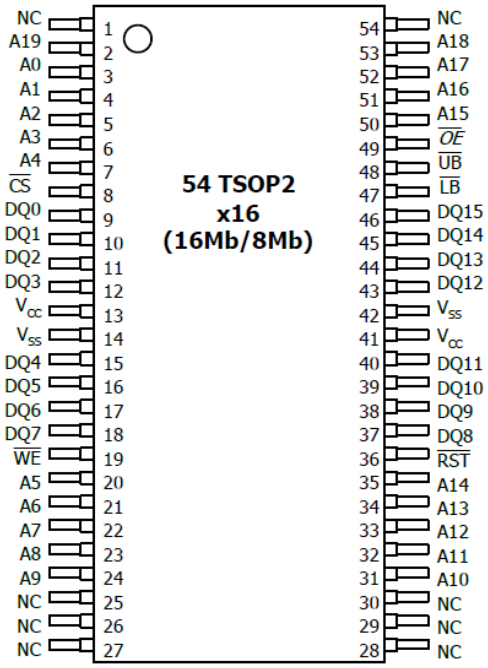
- Data Byte Control (x16 I/O Mode)
  - $\overline{LB}$: DQ7~DQ0, $\overline{UB}$: DQ15~DQ8
- Memory cell: STT-MRAM
  - nonvolatile
- Density
  - 16Mb, 8Mb, 4Mb, 2Mb and 1Mb
- Data Integrity: No external ECC required
- Data Endurance
  - Unlimited read cycle
  - 10^{14} write cycle
- Data Retention
  - 10 years at 85°C
- Single Power Supply Operation
- Operating Temperature Rang
  - Industrial Temperature: -40°C to 85°C
- RoHS compliant package
  - 44 TSOP2-400mil
  - 48 TFBGA-6x8mm
  - 54 TSOP2-400mil

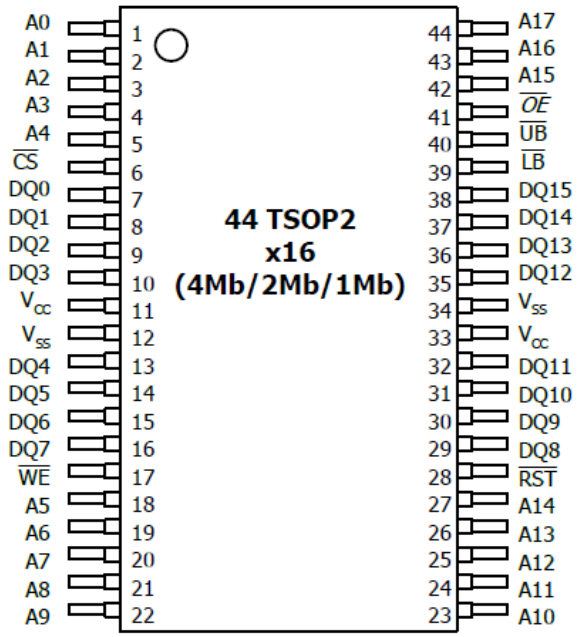
Pin Description – x16 I/O Mode

Figure 1: Functional Block Diagram – x16 I/O mode



Package Pin Configuration -x16 I/O Mode





48 Ball FBGA(16Mb~1Mb, x16)

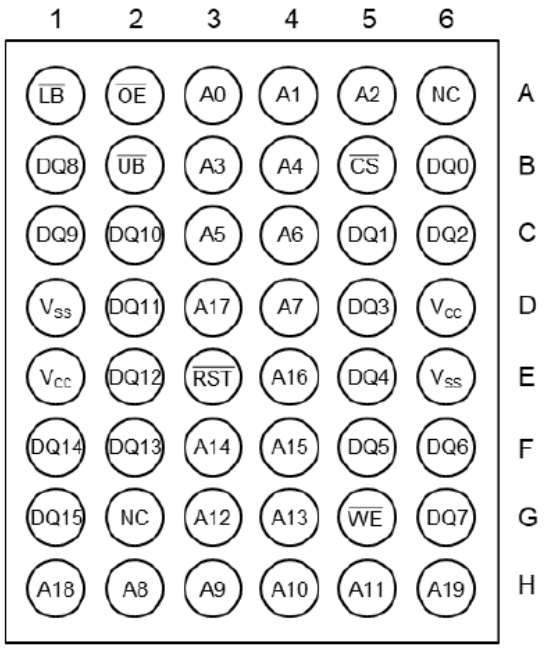


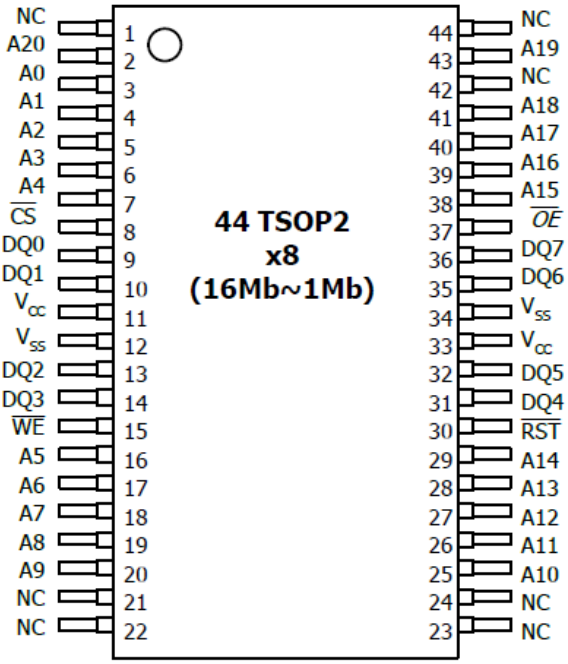
Table 1: DNU Pin Description – x16 I/O mode

Package	Density	DNU pin
54 TSOP2	8Mb	#2(A19)
44 TSOP2	2Mb	#44(A17)
	1Mb	#44(A17), #43(A16)
48 FBGA	8Mb	H6(A19)
	4Mb	H6(A19), H1(A18)
	2Mb	H6(A19), H1(A18), D3(A17)
	1Mb	H6(A19), H1(A18), D3(A17), E4(A16)

Table 2: Pin Description– x16 I/O mode

Pin	Type	Description
$\overline{CS}$	Input	**Chip Select:** When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored, and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
$\overline{WE}$	Input	**Write Enable:** When $\overline{CS}$ and $\overline{WE}$ are driven Low, write operation is initiated. The rising edge of $\overline{CS}$ causes the device to transfer the data to memory array. The rising edge of $\overline{WE}$ latches the input data. And the falling edge of $\overline{WE}$ latches a new page address for write cycles.
$\overline{OE}$	Input	**Output Enable**
$\overline{LB}$	Input	**Lower Byte Control:** DQ7~DQ0
$\overline{UB}$	Input	**Upper Byte Control:** DQ15~DQ8
A19~A0	Input	**Address** The LSB address A1~A0 are used for page mode read and write operation.
DQ15~DQ0	Bidirectional	Data Input/Outputs
$\overline{RST}$	Input	**Reset** $\overline{RST}$ pin is a hardware RESET signal. When $\overline{RST}$ is driven High, the device is in the normal operation mode. When $\overline{RST}$ is driven Low, the device enters in the initialization mode. This pin has an internal pullup resistor.
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use: DNUs must be left unconnected.

Package Pin Configuration -x8 I/O Mode



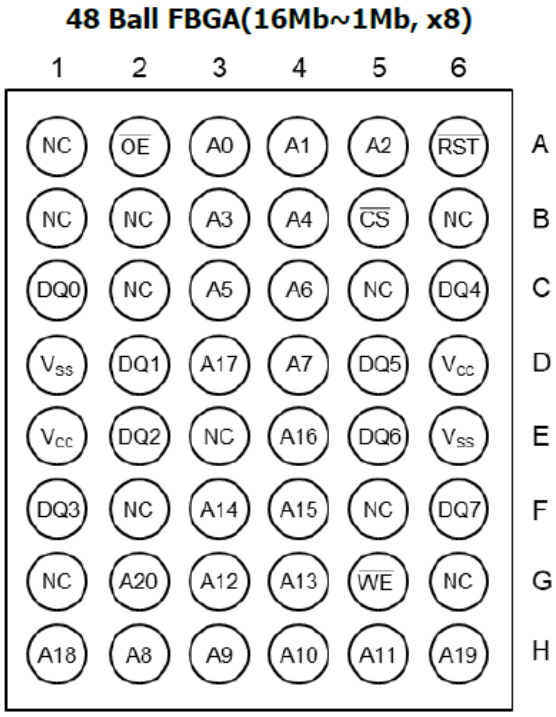


Table 3: Pin Description– x8 I/O mode

Package	Density	DNU pin
44 TSOP2	8Mb	#2(A20)
	4Mb	#2(A20), #43(A19)
	2Mb	#2(A20), #43(A19), #41(A18)
	1Mb	#2(A20), #43(A19), #41(A18), #40(A17)
48 FBGA	8Mb	G2(A20)
	4Mb	G2(A20), H6(A19)
	2Mb	G2(A20), H6(A19), H1(A18)
	1Mb	G2(A20), H6(A19), H1(A18), D3(A17)

Pin Description – x16 I/O Mode

Figure 1: Functional Block Diagram – x16 I/O mode

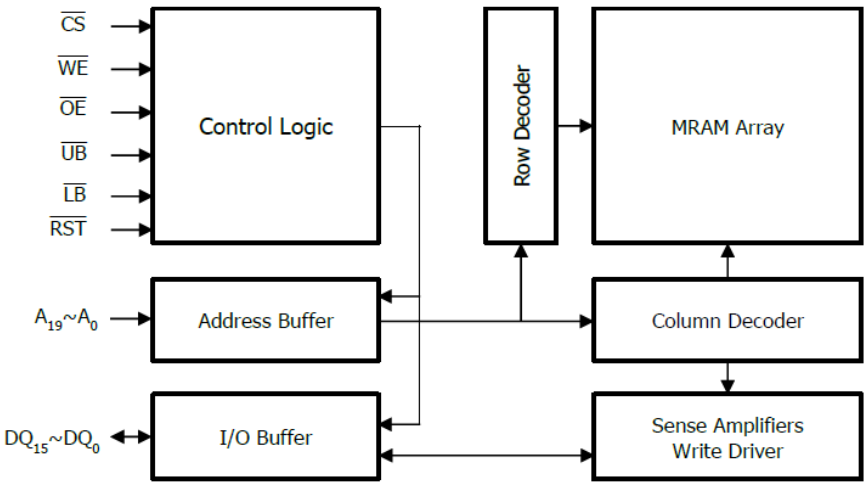


Table 4: Pin Description - x16 I/O mode

Pin	Type	Description
$\overline{CS}$	Input	**Chip Select:** When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored, and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
$\overline{WE}$	Input	**Write Enable:** When $\overline{CS}$ and $\overline{WE}$ are driven Low, write operation is initiated. The rising edge of $\overline{CS}$ causes the device to transfer the data to memory array. The rising edge of $\overline{WE}$ latches the input data. And the falling edge of $\overline{WE}$ latches a new page address for write cycles.
$\overline{OE}$	Input	**Output Enable**
$\overline{LB}$	Input	**Lower Byte Control:** DQ7~DQ0
$\overline{UB}$	Input	**Upper Byte Control:** DQ15~DQ8
A19~A0	Input	**Address** The LSB address A1~A0 are used for page mode read and write operation.
DQ15~DQ0	Bidirectional	Data Input/Outputs

$\overline{RST}$	Input	Reset $\overline{RST}$ pin is a hardware RESET signal. When $\overline{RST}$ is driven High, the device is in the normal operation mode. When $\overline{RST}$ is driven Low, the device enters in the initialization mode. This pin has an internal pullup resistor.
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use: DNUs must be left unconnected.

Pin Description – x8 I/O Mode

Figure 2: Functional Block Diagram – x8 I/O mode

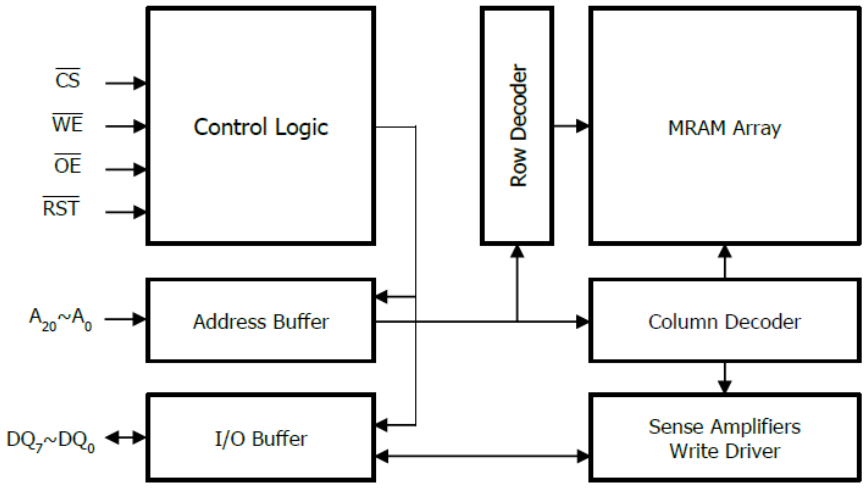


Table 5: Pin Description – x8 I/O mode

Pin	Type	Description
$\overline{CS}$	Input	**Chip Select:** When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored, and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
$\overline{WE}$	Input	**Write Enable:** When $\overline{CS}$ and $\overline{WE}$ are driven Low, write operation is initiated. The rising edge of $\overline{CS}$ causes the device to transfer the data to memory array. The rising edge of $\overline{WE}$ latches the input data. And the falling edge of $\overline{WE}$ latches a new page address for write cycles.
$\overline{OE}$	Input	Output Enable
A_{20}~A_0	Input	Address The LSB address A_2~A_0 are used for page mode read and write operation.
DQ_7~DQ_0	Bidirectional	Data Input/Outputs
$\overline{RST}$	Input	**Reset** $\overline{RST}$ pin is a hardware RESET signal. When $\overline{RST}$ is driven High, the device is in the normal operation mode. When $\overline{RST}$ is driven Low, the device enters in the initialization mode. This pin has an internal pullup resistor.
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use: DNUs must be left unconnected.

Functional Description

Functional Description – x16 I/O Mode

Table 6: Functional Description - x16 I/O mode

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ_7~DQ_0	DQ_{15}~DQ_8	Modes	Supply Current
H	X	X	X	X	High-Z	High-Z	Not Selected	I_{SB}
L	H	H	X	X	High-Z	High-Z	Output disable	I_{CCR}
L	H	L	H	H	High-Z	High-Z	Output disable	I_{CCR}
L	H	L	L	H	Dout	High-Z	Lower Byte Read	I_{CCR}
L	H	L	H	L	High-Z	Dout	Upper Byte Read	I_{CCR}
L	H	L	L	L	Dout	Dout	Word Read	I_{CCR}
L	L	X	H	H	High-Z	High-Z	Input disable	I_{CCW}
L	L	X	L	H	Din	High-Z	Lower Byte Write	I_{CCW}
L	L	X	H	L	High-Z	Din	Upper Byte Write	I_{CCW}
L	L	X	L	L	Din	Din	Word Write	I_{CCW}

Functional Description – x8 I/O Mode

Table 7: Functional Description - x8 I/O mode

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	DQ_7~DQ_0	Modes	Supply Current
H	X	X	High-Z	Not Selected	I_{SB}
L	H	H	High-Z	Output disable	I_{CCR}
L	H	L	Dout	Word Read	I_{CCR}
L	L	X	Din	Word Write	I_{CCW}

Address Pin

Table 8: Address Pin

Density	Address Pin x16 I/O mode	Address Pin x8 I/O mode
16Mb	A [19:0]	A [20:0]
8Mb	A [18:0]	A [19:0]
4Mb	A [17:0]	A [18:0]
2Mb	A [16:0]	A [17:0]
1Mb	A [15:0]	A [16:0]

Parameter	x16 I/O mode	x8 I/O mode
Page Address	A_1~A_0	A_2~A_0

Electrical Specifications

Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Parameter	Min.	Max.		Unit
		1.8V	3.3V	
Voltage on Vcc Supply Relative to VSS	-0.5	2.35	3.8	V
Voltage on Any Pin relative to VSS	-0.5	2.35	3.8	V
Storage Temperature	-55	150		°C
Operating Ambient Temperature	-40	85		°C
ESD HBM (Human Body Model)	≥ |2000 V|			V
ESD CDM (Charged Device Model)	≥ |500 V|			V
Solder Reflow Process	JEDEC J-STD-020 reflow profiles Peak temperature ≤ 260°C The time above 255°C ≤ 30 seconds Reflow cycles ≤ 3 times			

Endurance, Retention and Magnetic Immunity

Table 10: Endurance, Retention and Magnetic Immunity

Parameter	Conditions	Min.	Max.	Unit
Write Endurance	-25°C	10^{14}	-	Cycles/page
Data Retention	85°C	10	-	years
Magnetic Field During Write or Read	-	-	24,000	A/m

Recommended Operating Conditions

Table 11: Recommended Operating Conditions

Parameter / Condition	Min.		Typ.		Max.		Unit
	1.8V	3.3V	1.8V	3.3V	1.8V	3.3V	
Operating Temperature	-40		25		85		°C
Vcc Supply Voltage	1.71	2.7	1.8	3.3	1.98	3.6	V
Vss Supply Voltage	0.0		0.0		0.0		V

Pin Capacitance

Table 12: Pin Capacitance

Parameter	Conditions	Typ.	Max.	Unit
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	-	4	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; $V_{I/O}$ = 0V	-	6	pF

AC Test Condition

Table 13: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to Vcc
Input rise and fall times	1ns/1V
Input and output measurement timing levels	Vcc/2
Output Load	CL = 30pF

DC Characteristics

Table 14: DC Characteristics

Parameters		Symbol	Test Conditions	Min		Typ		Max		Unit
				1.8V	3.3V	1.8V	3.3V	1.8V	3.3V	
Input Leakage Current		I_{LI}	V_{IN} = V_{SS} to V_{CC}	-2		-		+2		uA
Output Leakage Current		I_{LO}	/CS=V_{IH} or /OE=V_{IH} or /WE=V_{IL} V_{OUT} = V_{SS} to V_{CC}	-2		-		+2		uA
Read Current	Random	I_{CCR}	V_{CC} (max), I_{OUT}=0mA	-		9	12	13	16	mA
	Page mode	I_{CCRP}	V_{CC} (max), I_{OUT}=0mA	-		9	12	13	16	mA
Write Current	Random	I_{CCW}	V_{CC} (max)	-		14	15	18	19	mA
	Page mode	I_{CCWP}	V_{CC} (max)	-		14	15	18	19	mA
Standby Current	16Mb	I_{SB}	V_{CC} (max), $\overline{CS}$≥V_{CC}-0.2V	-		300	350	450	490	uA
	1Mb~8Mb			-		185	250	330	370	uA
Input High Voltage		V_{IH}	-	0.7xV_{CC}		-		V_{CC}+0.3		V
Input Low Voltage		V_{IL}	-	-0.3		-		0.3xV_{CC}	0.2xV_C	V
Output High Voltage		V_{OH}	I_{OH}=-1mA	1.4	2.4	-		-		V
Output Low Voltage		V_{OL}	I_{OL}=2mA	-		-		0.4		V

AC Timing Parameters

Table 15: Read AC Timing Parameter

Parameter	Symbol	Min.	Max.	Unit
Read Cycle Time (Interpage)	t_{RC}	70	-	ns
Page Read Cycle Time (Intrapage)	t_{PRC}	15	-	ns
$\overline{CS}$ Read Active Time	t_{RCA}	65	-	ns
$\overline{CS}$ Falling to Valid Output Time	t_{CO}	-	65	ns
Address Access Time [2)]	t_{AA}	-	80	ns
Page Address Access Time	t_{PAA}	-	15	ns
$\overline{CS}$ Rising to Output Hold Time	t_{COH}	3	-	ns
Address change to Output Hold Time [2)]	t_{OH}	30	-	ns
Page address change to Output Hold Time	t_{POH}	5	-	ns
$\overline{OE}$ Falling to Valid Output Time	t_{OE}	-	15	ns

$\overline{UB}$, $\overline{LB}$ Falling to Valid Output Time [1)]	t_{BA}	-	15	ns
$\overline{CS}$ Rising to High-Z Output Time	t_{CHZ}	-	8	ns
$\overline{OE}$ Rising to High-Z Output Time	t_{OHZ}	-	8	ns
$\overline{UB}$, $\overline{LB}$ Rising to High-Z Output Time [1)]	t_{BHZ}	-	8	ns
Address Transition to $\overline{CS}$ falling Time [2)]	t_{CAS}	0	-	ns
$\overline{CS}$ Rising to Address Transition Time [2)]	t_{CAH}	0	-	ns
$\overline{WE}$ Rising to $\overline{CS}$ Falling Time	t_{WES}	0	-	ns
$\overline{CS}$ Rising to $\overline{WE}$ Falling Time	t_{WEH}	0	-	ns
$\overline{CS}$ High Time for Read End	t_{CSDR}	5	-	ns
Address Transition Interval Time	t_{AX}	-	5	ns

Notes: 1. Those parameters are applied for x16 I/O mode only. 2. Address except for page address

AC Timing Parameters

Table 16: Write AC Timing Parameter

Parameters	Symbol	Min	Max	Unit
Write Cycle Time (Interpage)	t_{WC}	320	-	ns
$\overline{CS}$ Write Active Time [3)]	t_{WCA}	20	-	ns
$\overline{CS}$ Falling to End of Write Time	t_{CW}	20	-	ns
Page Write Cycle Time (Intrapage)	t_{PWC}	15	-	ns
$\overline{WE}$ Falling to End of Write (invalid output does not appear)	t_{WP}	10	-	ns
$\overline{WE}$ Falling to End of Write (invalid output appears)	t_{WP1}	20	-	ns
$\overline{UB}$, $\overline{LB}$ Falling to End of Write Time [1)]	t_{BW}	10	-	ns
$\overline{WE}$ Falling to Output High-Z Time	t_{WHZ}	-	8	ns
Valid Input Data to End of Write Time	t_{DS}	8	-	ns
End of Write to Valid Input Data Time	t_{DH}	0	-	ns
Address Transition Time to $\overline{CS}$ falling [2)]	t_{CAS}	0	-	ns
$\overline{CS}$ Rising to Address Transition Time [2)]	t_{CAH}	0	-	ns
Page Address Transition to$\overline{WE}$ falling Time	t_{PAS}	0	-	ns
$\overline{WE}$ falling to Page Address Transition Time	t_{PAH}	10	-	ns
$\overline{WE}$ High Time for Page Write	t_{PWH}	3	-	ns
$\overline{CS}$ High Time for Write End [3)]	t_{CSDW}	250	-	ns

Notes: 1. Those parameters are applied for x16 I/O mode only. 2. Address except for page address 3. tWCA + tCSDW ≥ tWC

Power On/Off Sequence

- When power-up, power-down or power-loss, $\overline{CS}$ must follow Vcc to provide data protection.
- It is recommended that $\overline{CS}$ must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
- A 10KΩ pull-up resistor between Vcc and $\overline{CS}$ pin is recommended.
- Reset operation is required after t_{PU}.
- Normal operation must start after t_{RST}.

Figure 3: Power-Up/Down Behavior

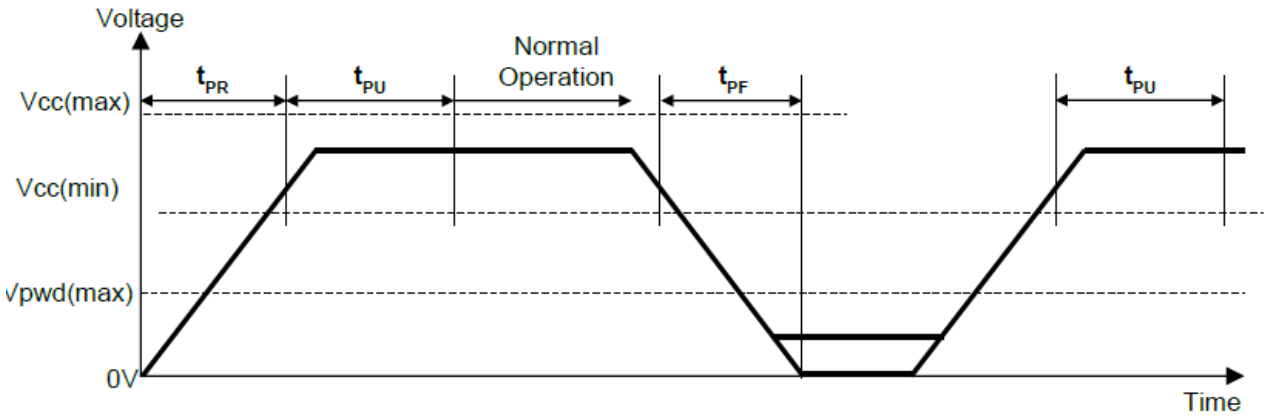


Table 17: Power-Up/Down Timing

Parameter	Symbol	Min		Max		Unit
		1.8V	3.3V	1.8V	3.3V	
Vcc Range	Vcc	1.71	2.7	1.98	3.6	V
Vcc rising time	t_{PR} (1)	30		-		µs/V
Vcc falling time	t_{PF} (1)	30		-		µs/V
Vcc(min) to $\overline{CS}$ Low (first instruction) time	t_{PU} (1)	1.0	2.0	-		ms
Vcc needed to below Vpwd for ensuring initialization will occur	V_{PWD}(1)	-		0.8	1.6	V

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

Device Operation

Read Operation: Interpage

Read operation is initiated when $\overline{CS}$ goes to low and $\overline{WE}$ high. The falling edge of $\overline{CS}$ latches the address and starts to read data from memory array. The output data are available after t_{CO}. The minimum random read cycle time is t_{RC}. The data remains in High-Z until the valid data is output.

Figure 4: Timing Waveform of Read Cycle: x16 I/O mode

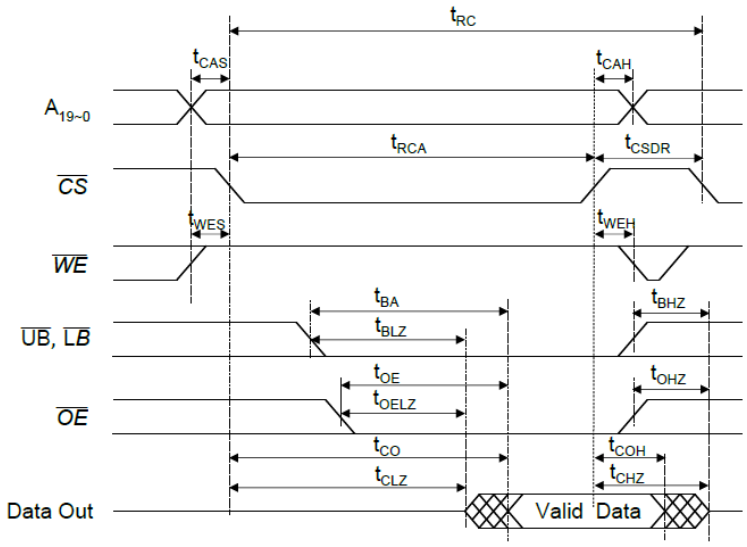
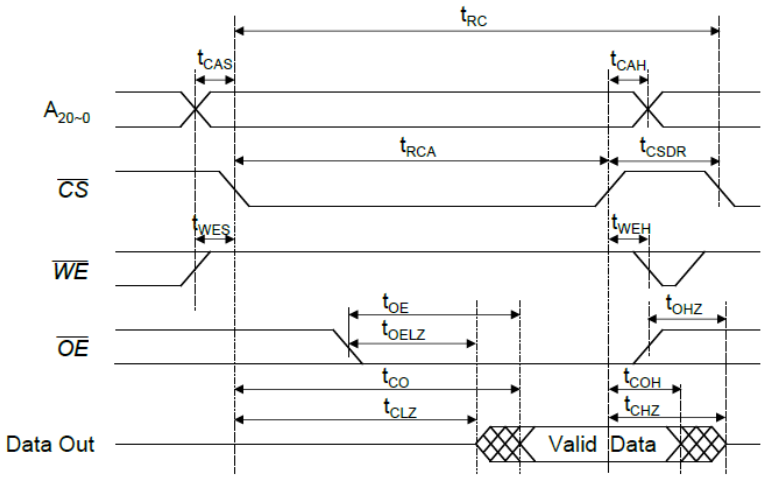


Figure 5: Timing Waveform of Read Cycle: x8 I/O mode



Page Mode Read Operation: Intrapage

The device supports the page mode read function to enhance the read performance. It reads a page data from memory array and latches the data into an internal page buffer.

The first data is output after t_{CO}. When the next page address is input, subsequent data is output from the page buffer after t_{PAA}.

The sequence and length of page address are not restricted. For example, the sequence A2-A0-A1 is available.

Table 18: Page Mode

Parameter	x16 I/O mode	x8 I/O mode
Page Address	A_1~A_0	A_2~A_0
Page size	4-word (8-bytes)	8-word (8-bytes)

Figure 6: Timing Waveform of Page Mode Read Cycle: x16 I/O mode

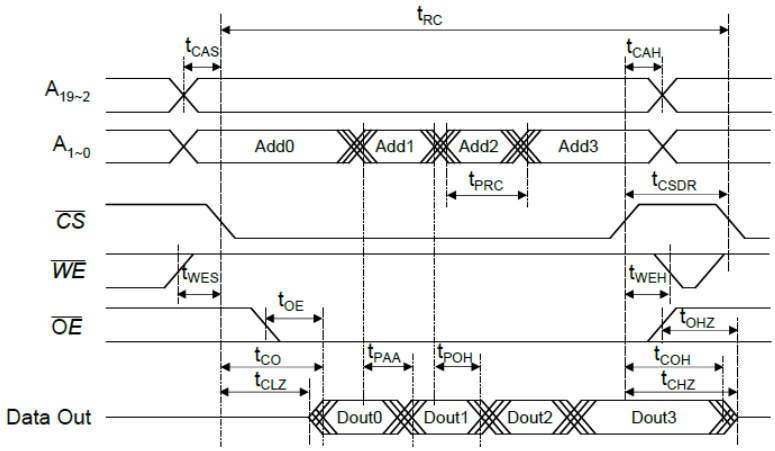
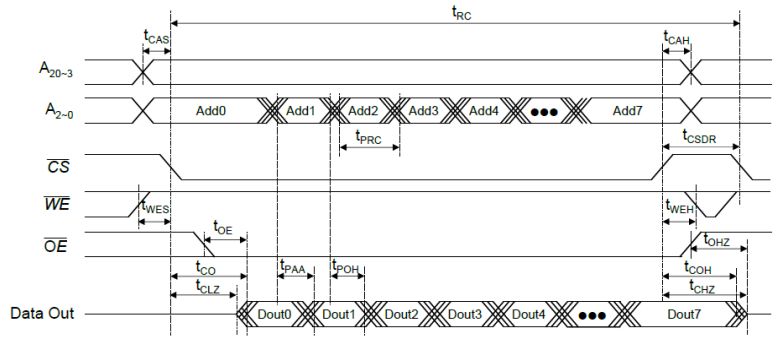


Figure 7: Timing Waveform of Page Mode Read Cycle: x8 I/O mode



Address Access Read Operation

During $\overline{CS}$ is low and $\overline{WE}$ is high, if a random address (except for the page address) are changed, the device reads a page data from memory array of a new address and latches the data into an internal page buffer. The first data is output after t_{AA}. When the next page address is input, subsequent data is output from the page buffer after t_{PAA}. The random address transition time should not exceed t_{AX}.

Figure 8: Timing Waveform of Address Access Read Cycle: x16 I/O mode

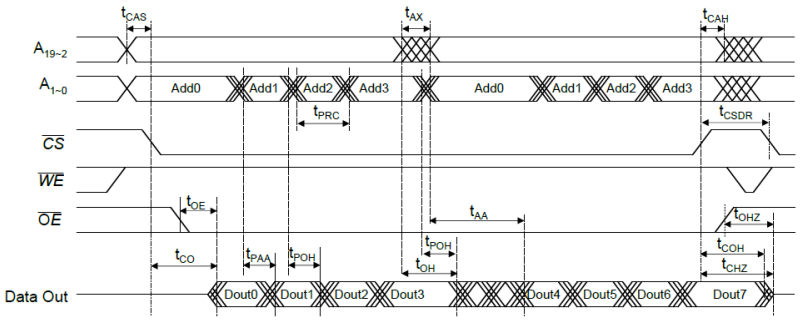
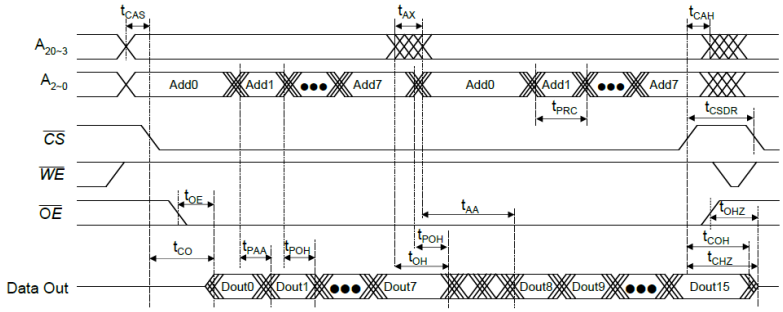


Figure 9: Timing Waveform of Address Access Read Cycle: x8 I/O mode



Write Operation ($\overline{WE}$ control): Interpage

Write operation is initiated when $\overline{WE}$ goes to low and $\overline{CS}$ is low. The device latches address on the falling edge of $\overline{CS}$. It latches the lower byte data on the rising edge of $\overline{WE}$ or $\overline{LB}$ and the upper byte data on the rising edge of $\overline{WE}$ or $\overline{UB}$ for x16 I/O mode. It latches the data on the rising edge of $\overline{WE}$ for x8 I/O mode. The rising edge of $\overline{CS}$ causes the device to transfer the input data to memory array.

Figure 10: Timing Waveform of Write Cycle ($\overline{WE}$ control): x16 I/O mode

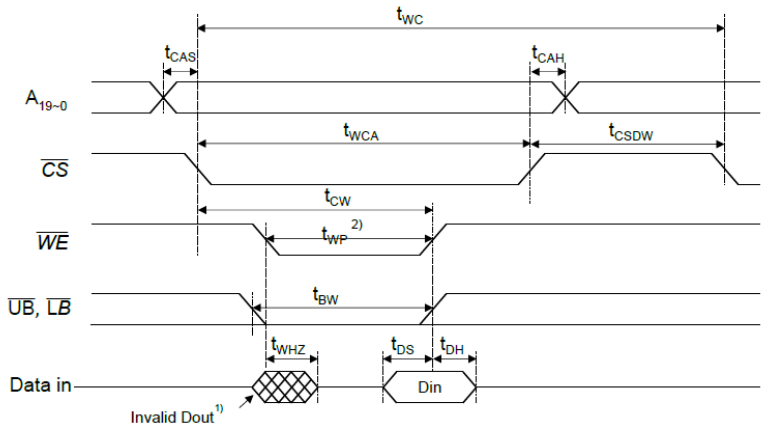
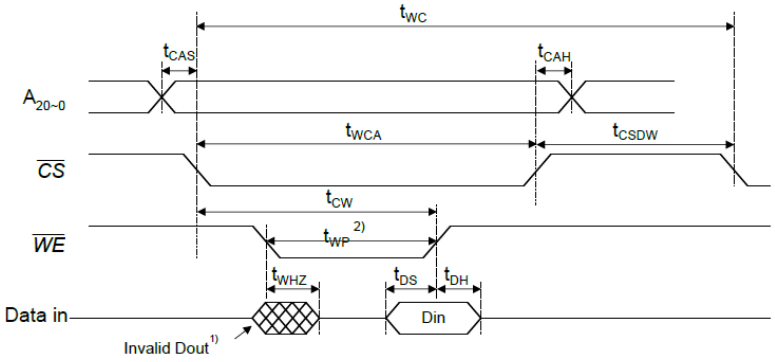


Figure 11: Timing Waveform of Write Cycle ($\overline{WE}$ control): x8 I/O mode



Notes:

1. The data pins remain in High-Z state if the time of $\overline{CS}$ falling to $\overline{WE}$ falling is smaller than 30ns or $\overline{OE}$ is High.

2. In case that the data pins do not remains in High-Z state, tWP should be tWP1

3. tWCA + tCSDW ≥ tWC

Write Operation ($\overline{CS}$ control): Interpage

Write operation is initiated when $\overline{CS}$ goes to low and $\overline{WE}$ is low. The device latches address on the falling edge of $\overline{CS}$. It latches the lower byte data on the rising edge of $\overline{CS}$ or $\overline{LB}$ and the upper byte data on the rising edge of $\overline{CS}$ or $\overline{UB}$ for x16 I/O mode.

It latches the data on the rising edge of $\overline{CS}$ for x8 I/O mode.

The rising edge of $\overline{CS}$ causes the device to transfer the input data to memory array.

Figure 12: Timing Waveform of Write Cycle ($\overline{CS}$ control): x16 I/O mode

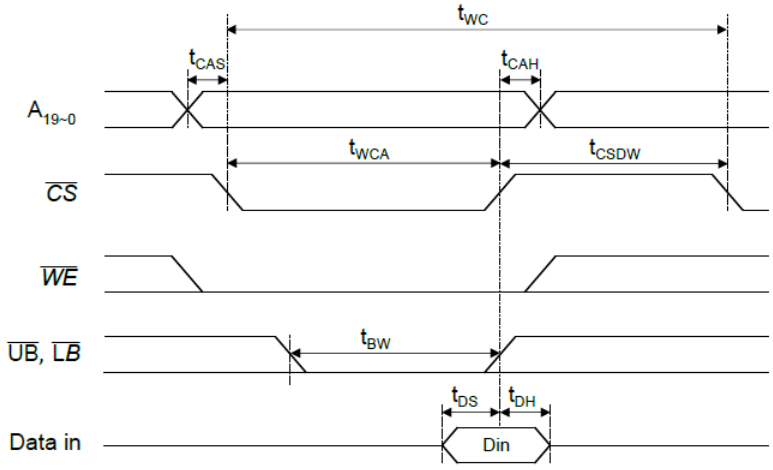
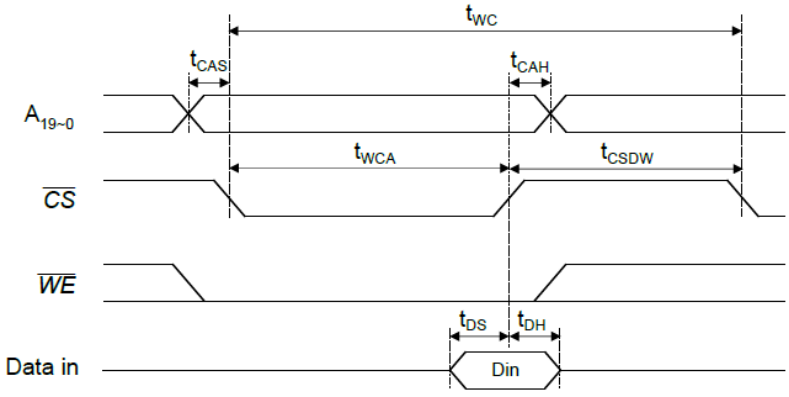


Figure 13: Timing Waveform of Write Cycle ($\overline{CS}$control): x8 I/O mode



Page Mode Write Operation: Intrapage

The device supports the page mode write function to enhance the write performance. It latches a page address every falling edge of $\overline{WE}$. It latches the lower byte data on every rising edge of $\overline{WE}$ or $\overline{LB}$ and the upper byte data on every rising edge of $\overline{WE}$ or $\overline{UB}$ for x16 I/O mode. It latches the data on every rising edge of $\overline{WE}$ for x8 I/O mode. The rising edge of $\overline{CS}$ causes the device to transfer the input data to memory array. The sequence and length of page address are not restricted. For example, the sequence A2-A0-A1 is available.

Figure 14: Timing Waveform of Page Mode Write Cycle: x16 I/O Mode

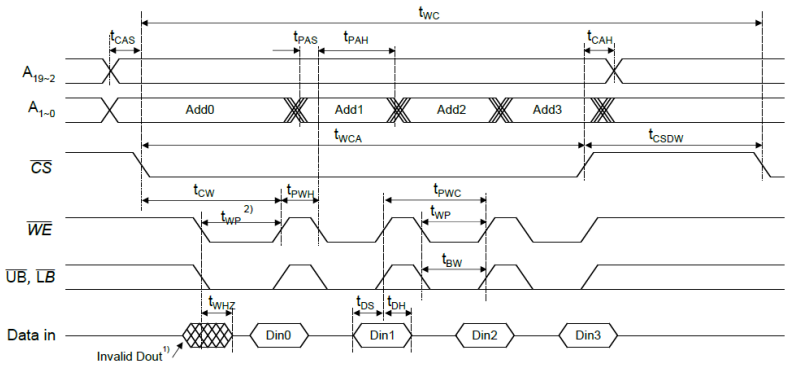
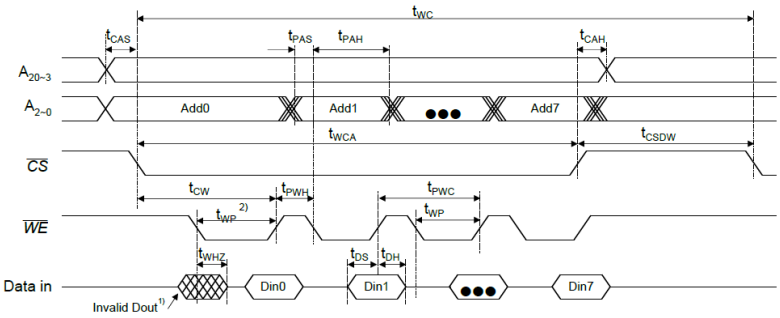


Figure 15: Timing Waveform of Page Mode Write Cycle: x8 I/O Mode



Note:

- While $\overline{CS}$ is Low, once $\overline{WE}$ goes to Low, output remains in High-Z state even if $\overline{WE}$ goes to High thereafter.

Thermal Resistance

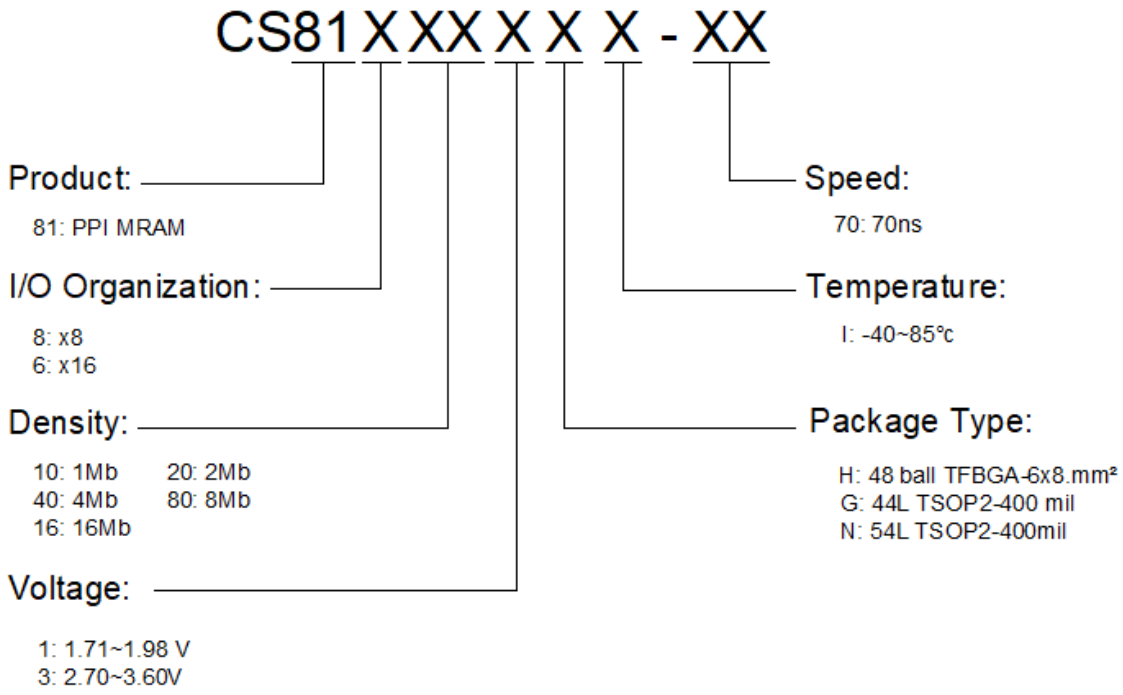
Table 19: Thermal Resistance

Parameter	Description	48FBGA	54TSOP2	44TSOP2	Unit
θ_{JA}	Thermal resistance (junction to ambient)	69.4	50.3	65.2	°C/W
θ_{JC}	Thermal resistance (junction to case)	31.1	14.4	15.9	

Notes:

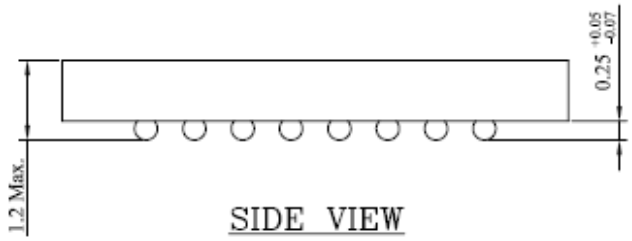
1: These parameters are guaranteed by characterization; not tested in production

Ordering Information

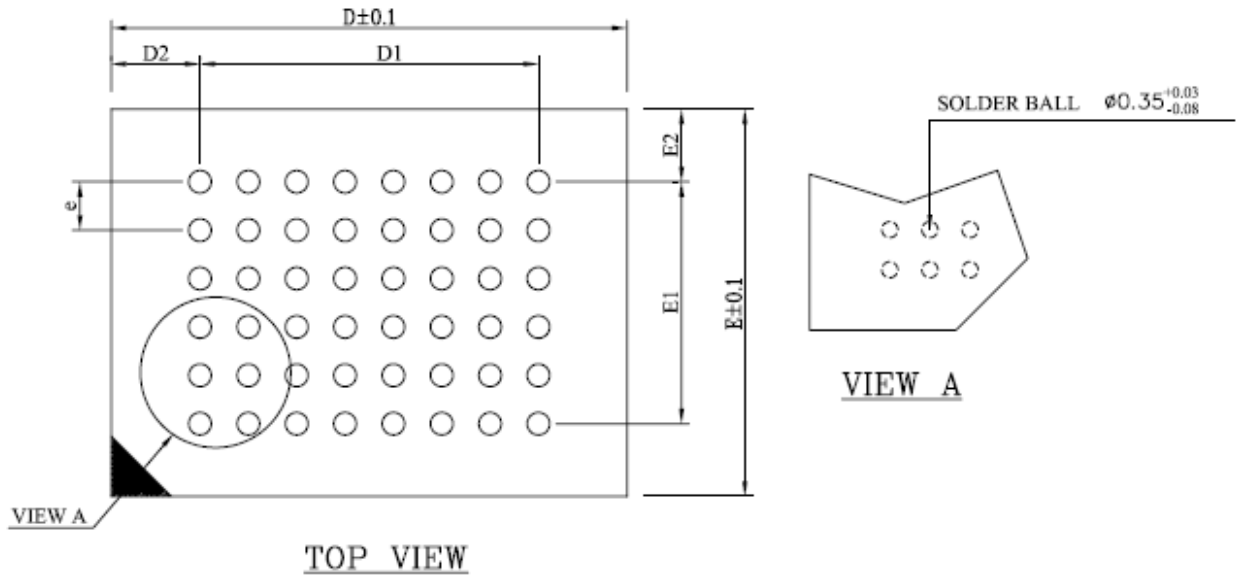


Package Outline

48 balls TFBGA-6x8mm



BALL PITCH e=0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125

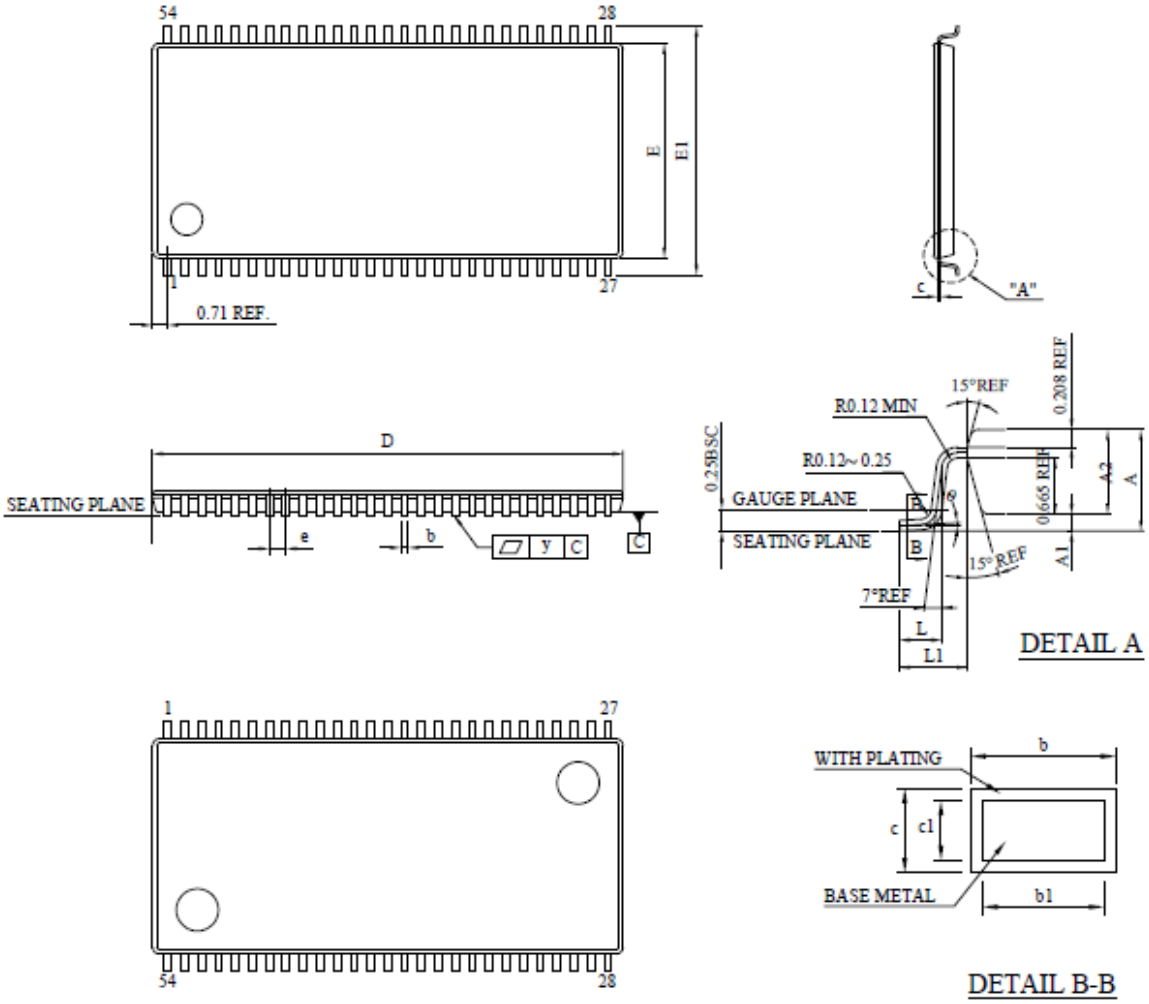


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:

LINEAR : X.X = ±0.1
X.XX = ± 0.05
X.XXX = ± 0.025

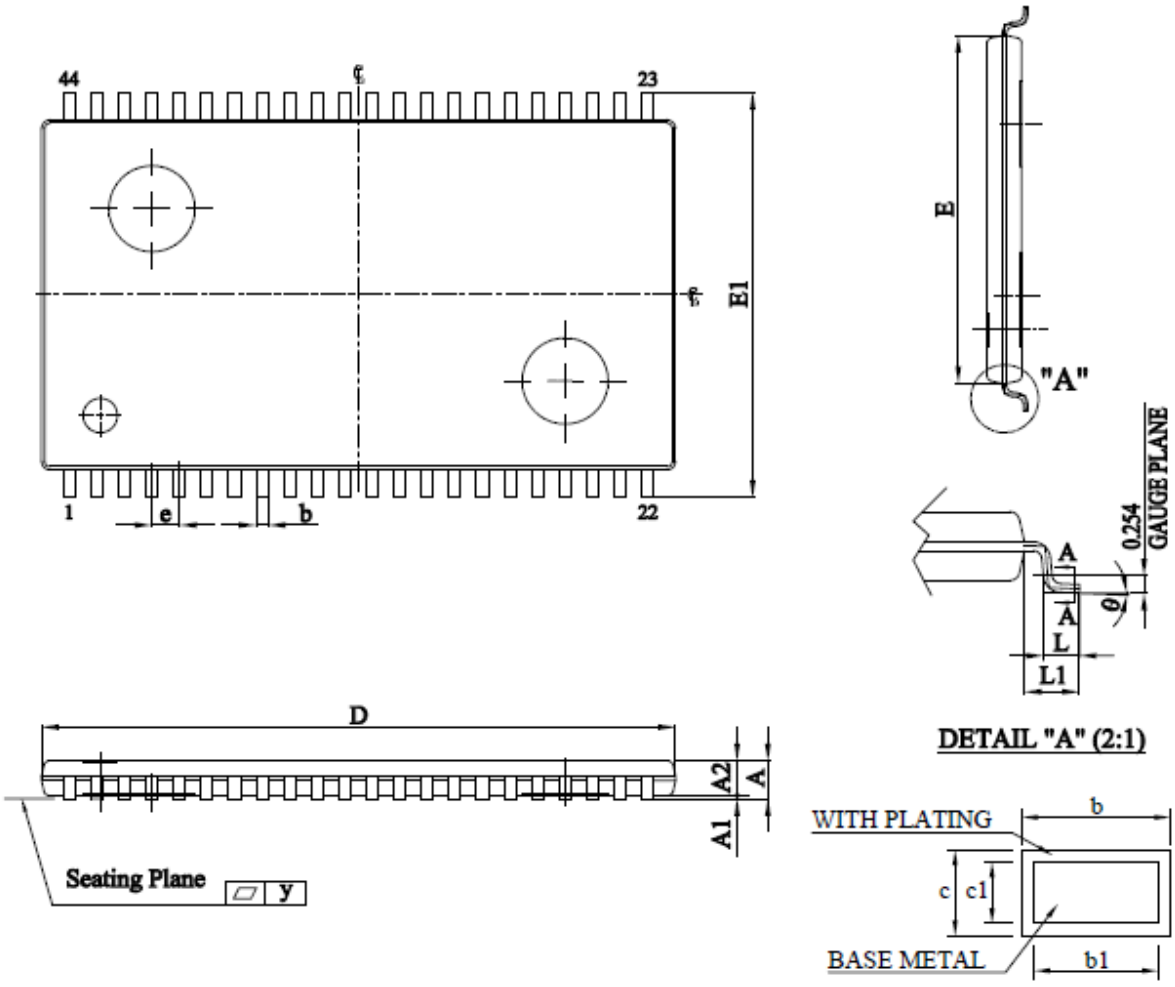
54L TSOP(II)-400 mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
mm	Min.	-	0.05	0.95	0.30	0.30	0.12	0.12	22.12	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	-	0.10	1.00	–	–	–	–	22.22	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	22.32	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	-	0.002	0.037	0.012	0.012	0.005	0.005	0.871	0.396	0.455	0.028	0.016	0.028	–	0°
	Nom.	-	0.004	0.039	–	–	–	–	0.875	0.400	0.463	0.031	0.020	0.031	–	–
	Max.	0.047	0.006	0.041	0.018	0.016	0.008	0.006	0.879	0.404	0.471	0.035	0.024	0.035	0.004	8°

44L TSOP(II)-400 mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°