



Low Power Pseudo SRAM

2M word x 16 bit

CS26LV32173

Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20180019	5/29-2018	New issue	Hank Lin
2.0	20180021	10/1-2018	Revise timing waveform of power up	Hank Lin
3.0	20200018	12/7-2020	Revise Read /Write Timing Charts	Hank Lin
4.0	20210025	6/24-2021	Revise V _{CC} range from 2.7~3.6V to 2.7~3.3V	Hank Lin
5.0	20260001	12/29-2025	Revise V _{CC} range from 2.7~3.3V to 2.6~3.3V	Hank Lin



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■ Product Description

The CS26LV32173 is a 32M-bit PSRAM organized as 2M words by 16 bits. It provides high density, high speed and low power. The device operates single power supply. The device also features SRAM-like W/R timing whereby the device is controlled by /CE, /OE and /WE on asynchronous. The device has realizing low-power standby. The CS26LV32173 is available die form and 48-Ball TFBGA packages.

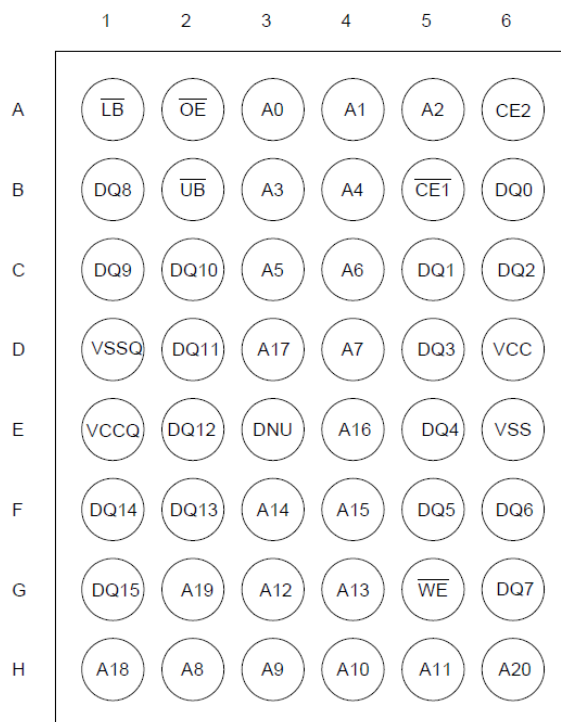
■ Features

- Single power supply voltage of 2.6 to 3.3V
- Direct TTL compatibility for all inputs and outputs.
- Deep power-down mode: Memory cell data invalid.
- Page operation mode
- Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
 - Standby 120 uA(Max)
 - Deep power-down standby 15 uA (Max.)
- Access Time
 - /CE1 Access Time: 70ns
 - /OE Access Time: 25ns
 - Page Access Time: 25ns

■ Product Family

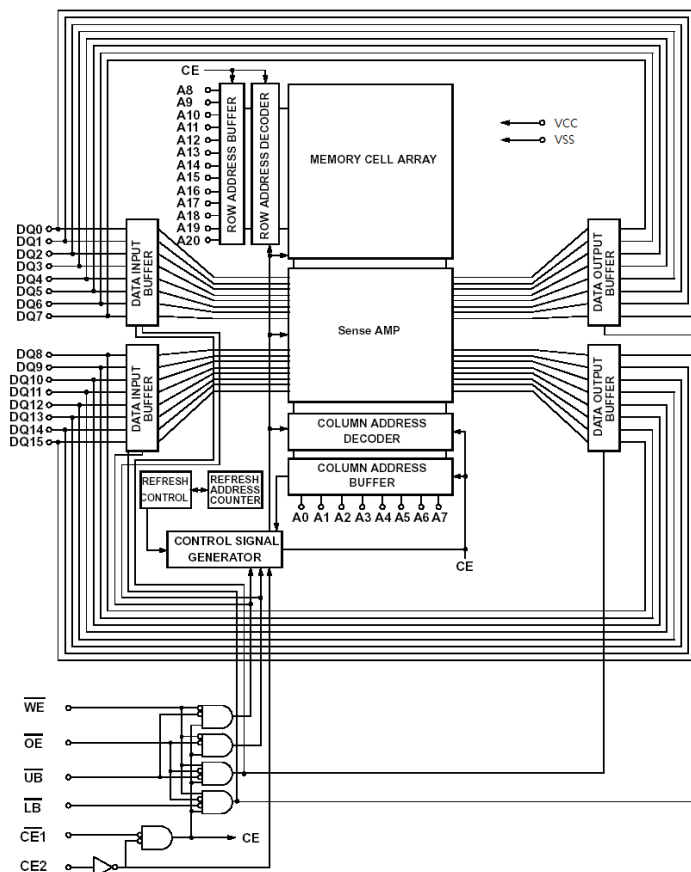
Product Family	Operating Temp	Vcc. Range	Speed(ns)	Standby (Max.)	Package Type
CS26LV32173	0~70°C	2.6~3.3	70	120 uA	48ball TFBGA-6*8mm
	-40~85°C				

■ Pin Configuration



48 TFBGA - Top View

■ Functional Block Diagram



Pin Descriptions

Name	Type	Function
A0~A20	input	Address input
CE1	input	Chip Enable Input1, Low : Enable
CE2	input	Chip Enable Input2, High: Enable, Low: Enter Power Down mode
/WE	input	Write Enable input, Low :Enable
/OE	input	Output Enable input, Low :Enable
/LB	input	Lower byte write control
/UB	input	Upper byte write control
DQ0~DQ15	I/O	Data inputs/outputs
V _{CC}	Power	Device Power supply
V _{SS}	Power	V _{SS} must be connected ground
V _{CCQ}	Power	I/O Power supply
V _{SSQ}	Power	V _{SSQ} must be connected ground
DNU		Do not use

Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V _{CC} Current
Standby	H	H	X	X	X	X	High Z	High Z	I _{CCSB} , I _{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I _{CC}
Read	L	H	L	H	L	L	D _{OUT}	D _{OUT}	I _{CC}
Upper Byte Read					L	H	D _{OUT}	High Z	I _{CC}
Lower Byte Read					H	L	High Z	D _{OUT}	I _{CC}
Write	L	H	H	L	L	L	D _{IN}	D _{IN}	I _{CC}
Upper Byte Write					L	H	D _{IN}	Invalid	I _{CC}
Lower Byte Write					H	L	Invalid	D _{IN}	I _{CC}

Note: X means don't care. (Must be low or high state)

Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Rating	Unit
V _{IN}	Input Voltage	-0.2 to V _{CC} +0.3	V
V _{OUT}	Output Voltage	-0.2 to V _{CC} +0.3	
V _{CC}	Device Power Supply Voltage	-0.2 to 3.3	V
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Operating Temperature	-40 to +85	°C
P _D	Power Dissipation	1.0	W

1. Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device.

Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Recommended DC Operating Conditions

($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.0\text{V}$)

Item	Symbol	CS26LV16173			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	2.6	3.0	3.3	V
I/O operating voltage ($V_{CCQ} \leq V_{CC}$)	V_{CCQ}	2.6	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	$0.7V_{CCQ}$	V_{CC}	$V_{CC}+0.2^{(1)}$	V
Input low voltage	V_{IL}	$-0.2^{(2)}$	0	$0.2V_{CCQ}$	V

Note :

1. Overshoot : $V_{CC}+1.0\text{V}$ in case of pulse width $\leq 20\text{ns}$.
2. Undershoot : -1.0V in case of pulse width $\leq 20\text{ns}$.
3. Overshoot and undershoot are sampled, not 100% tested.

■ DC and Operating Characteristics

Item	Symbol	Test Conditions	Min.	Typ	Max.	unit
Input leakage current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}	-1	-	1	μA
Output leakage current	I_{LO}	$/CS=V_{IH}$, $/ZZ=V_{IH}$, $/OE=V_{IH}$ or $/WE=V_{IL}$, $V_{IO}=V_{SS}$ to V_{CC}	-1	-	1	μA
Average operating current	I_{CC1}	Cycle time=1 μs , 100%duty, $I_{IO}=0\text{mA}$, $/CS \leq 0.2\text{V}$, $/ZZ=V_{IH}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	-	-	3	mA
	I_{CC2}	Cycle time=Min, $I_{IO}=0\text{mA}$, 100% duty, $/CS=V_{IL}$, $/ZZ=V_{IH}$, $V_{IN}=V_{IL}$ or V_{IH}	-	-	20	mA
Page mode operating current	I_{CCP}	Cycle time=Min (t_{RC} , t_{PC}), $I_{IO}=0\text{mA}$, 100% duty, $/CS=V_{IL}$, $/ZZ=V_{IH}$, $V_{IN}=V_{IL}$ or V_{IH}	-	-	15	mA
Output low voltage	V_{OL}	$I_{OL}=0.5\text{mA}$			0.2^* V_{CCQ}	V
Output high voltage	V_{OH}	$I_{OH}=-0.5\text{mA}$	0.8^* V_{CCQ}			V
Standby Current(TTL)	I_{SB}	$/CS=V_{IH}$, $/ZZ=V_{IH}$, Other inputs= V_{IH} or V_{IL}	-	-	0.3	mA
Standby Current(CMOS)	I_{SB1}	$/CS \geq V_{CC}-0.2\text{V}$, $/ZZ \geq V_{CC}-0.2\text{V}$, Other inputs= $0 \sim V_{CC}$	-	-	120	μA
Deep Power Down Modes	I_{SB0}	$/ZZ \leq 0.2\text{V}$, Other inputs= $0 \sim V_{CC}$, No refresh(DPD)	-	-	15	μA

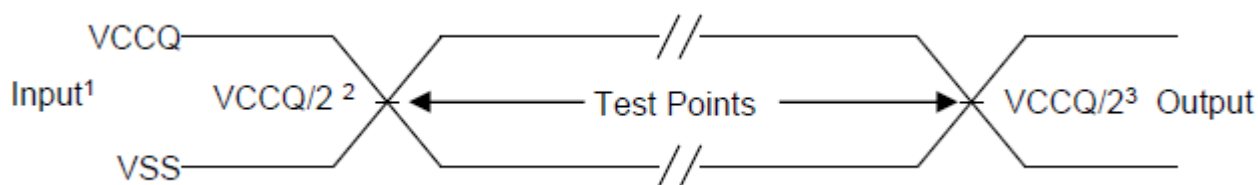
■ Capacitance⁽¹⁾

(TA = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Min.	MAX.	Unit
C _{IN}	Input Capacitance	V _{IN} =0V	2	5	pF
C _{OUT}	Output Capacitance	V _{OUT} =0V	3.5	5	pF

1. This parameter is sampled periodically and is not 100% tested

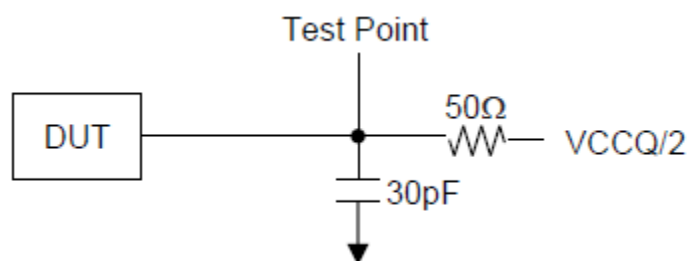
■ AC Input/Output Reference Waveform



NOTE:

1. AC test inputs are driven at V_{CCQ} for a logic 1 and VSS for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at V_{CCQ}/2.
3. Output timing ends at V_{CCQ}/2.

■ AC Test Conditions



■ AC Characteristics

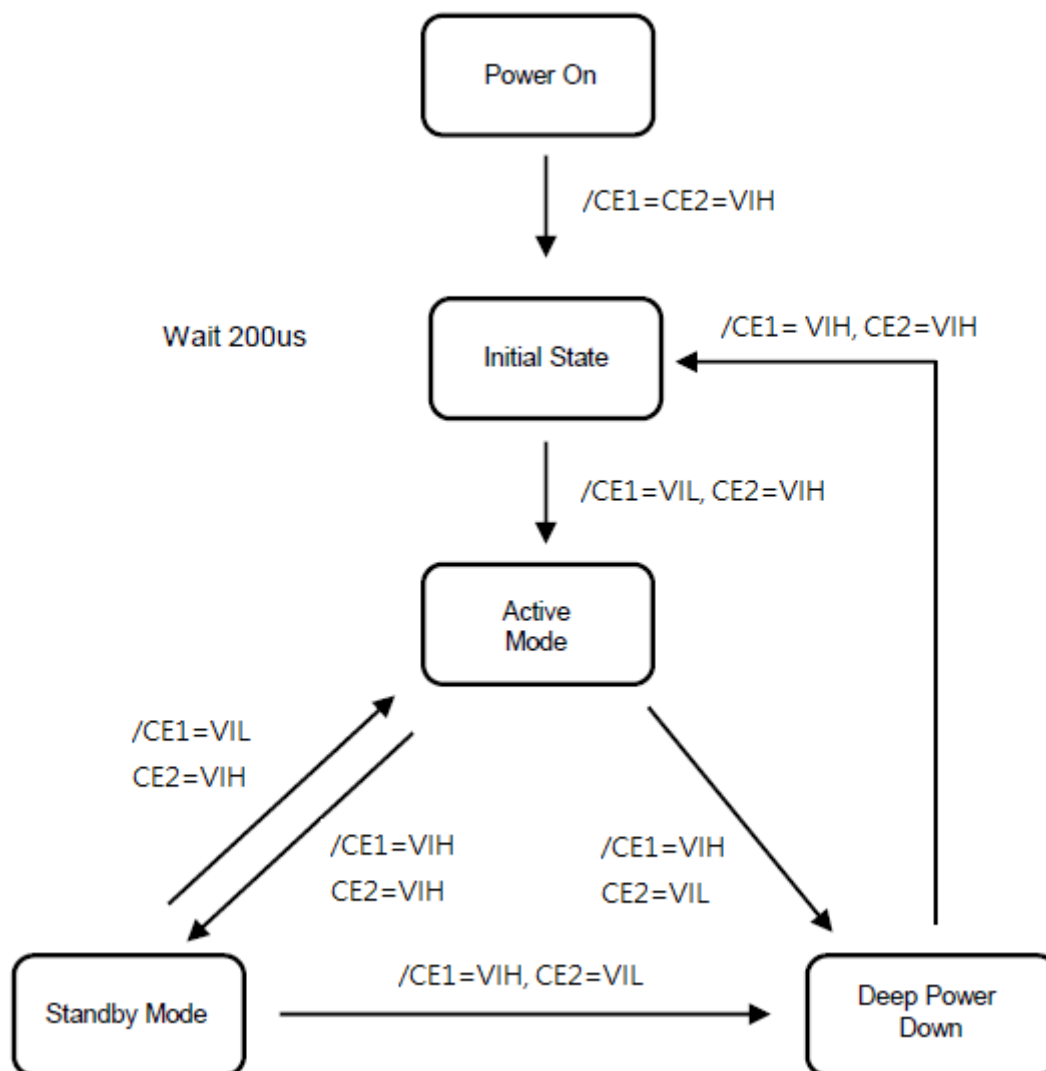
(V_{CC}=2.6V~3.3V, Commercial product: T_A = 0 to + 70°C , Industrial product : T_A=-40 to 85°C)

Parameter List		Symbol	70ns		Units
			Min	Max	
Read	Read Cycle Time	t _{RC}	70	-	ns
	Address Access Time	t _{AA}	-	70	ns
	Chip Select to Output	t _{CO}	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	20	ns
	/UB, /LB Access Time	t _{BA}	-	25	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	ns
	/UB, /LB Enable to Low-Z Output	t _{BLZ}	0	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	0	-	ns
	Chip Disable to High- Z Output	t _{HZ}	0	8	ns
	/UB, /LB Disable to High- Z Output	t _{BHZ}	0	8	ns
	Output Disable to High- Z Output	t _{OHZ}	0	8	ns
	Output Hold from Address Change	t _{OH}	5	-	ns
Write	Write Cycle Time	t _{WC}	70	20k	ns
	Chip Select to End of Write	t _{CW}	60	-	ns
	Address Set-up Time	t _{AS}	0	-	ns
	Address Valid to End of Write	t _{AW}	60	-	ns
	/UB, /LB Valid to End of Write	t _{BW}	60	-	ns
	Write Pulse Width	t _{WP}	50	-	ns
	Write Recovery Time	t _{WR}	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	8	ns
	Data to Write Time Overlap	t _{DW}	20	-	ns
	Data Hold from Write Time	t _{DH}	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	ns
Page	Page Mode Cycle Time	t _{PC}	25	-	ns
	Page Mode Address Access Time	t _{PAA}	-	25	ns
	Maximum Cycle Time	t _{MRC}	-	20k	ns
/CS High Pulse Width		t _{CP}	10	-	ns

■ Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CE1=CE2=VIH

■ Standby Mode State machines

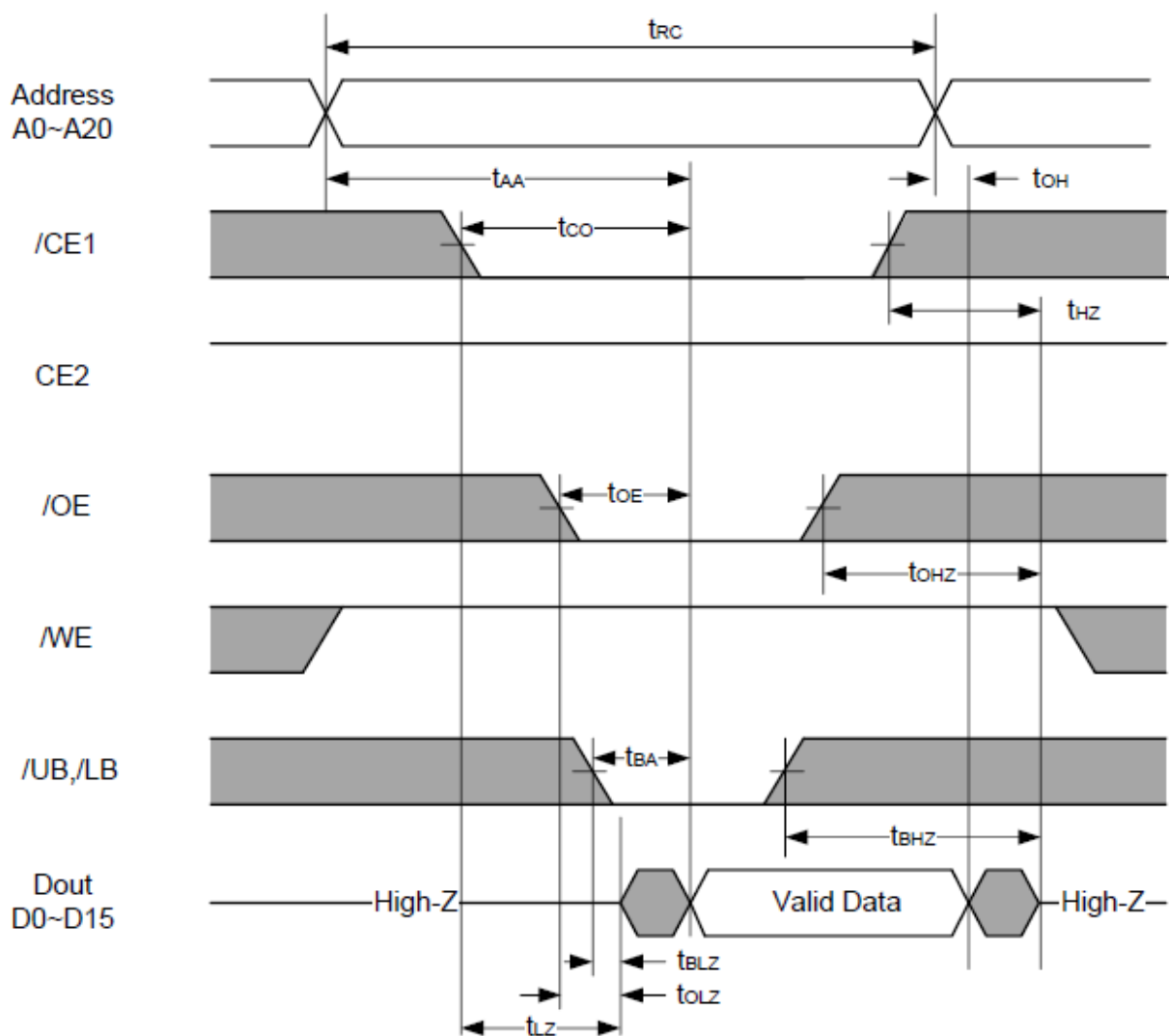


■ Standby Mode Characteristics

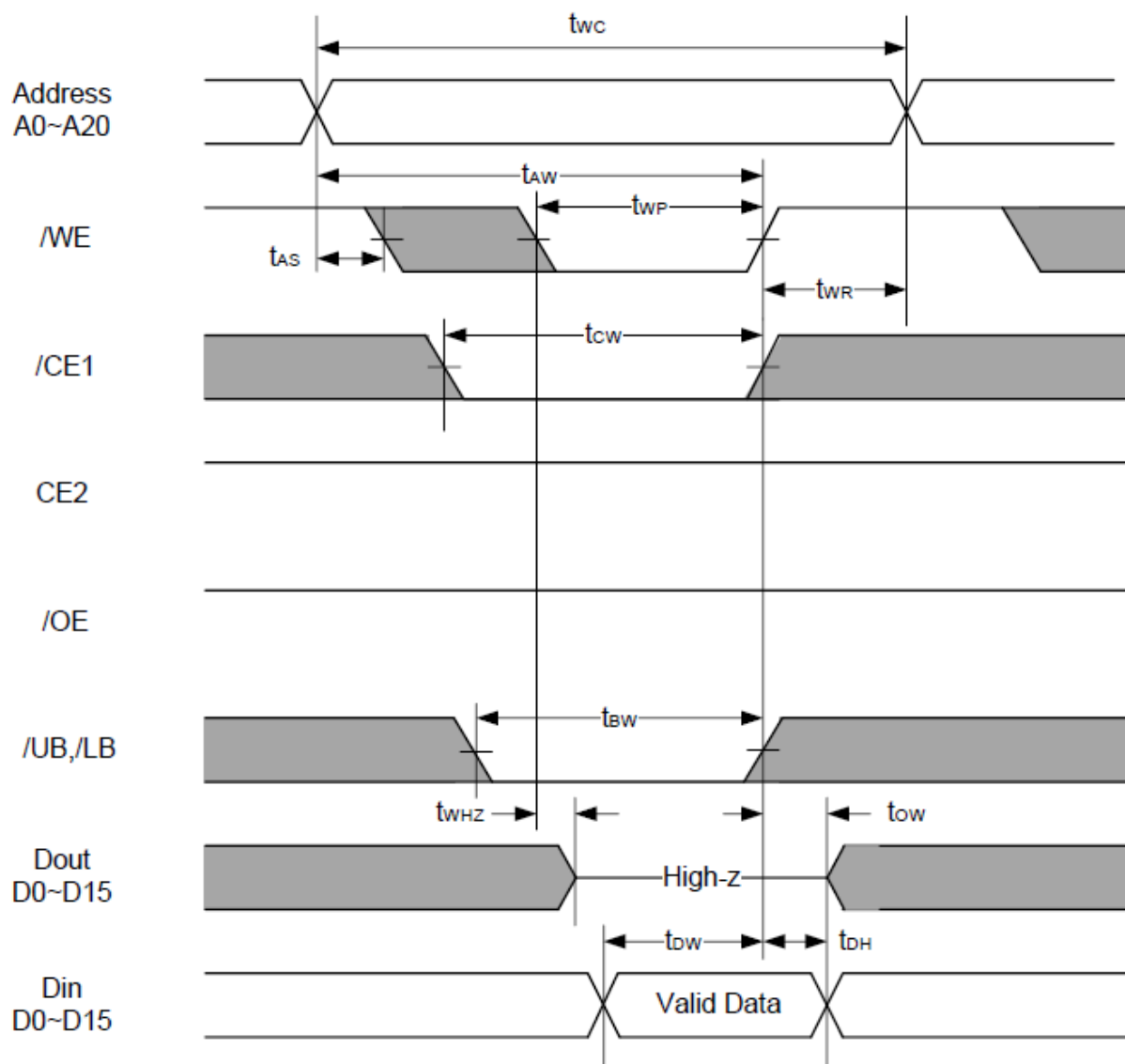
Mode	Memory Cell Data	Standby Current(μA)	Wait Time(us)
Standby	Valid	120 (ISB1)	0
Deep Power Down	Invalid	15 (ISB0)	200

■ Timing Diagrams

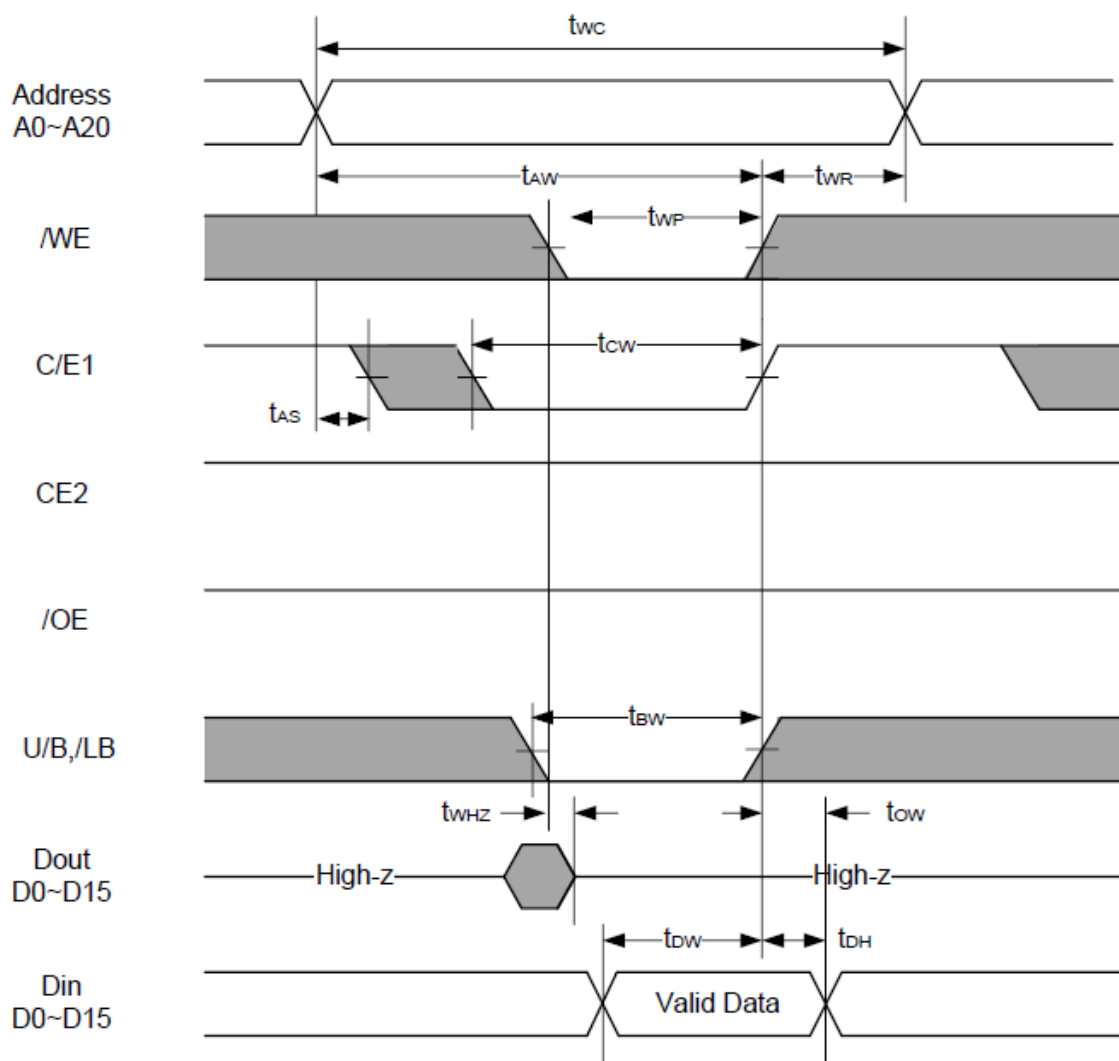
<Read Cycle>



Write Cycle (1) (/WE controlled)



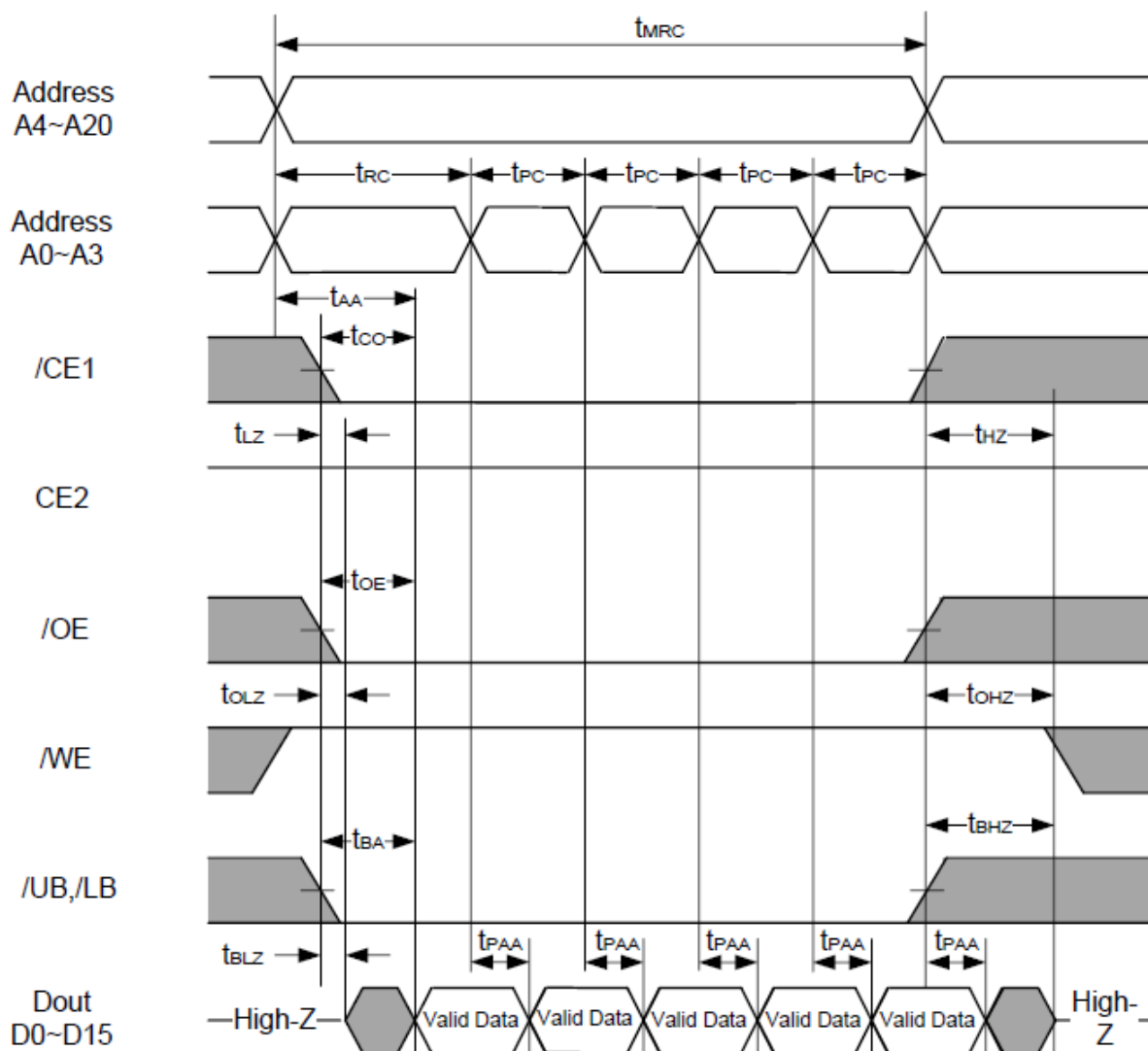
Write Cycle (2) (/CE1 controlled)



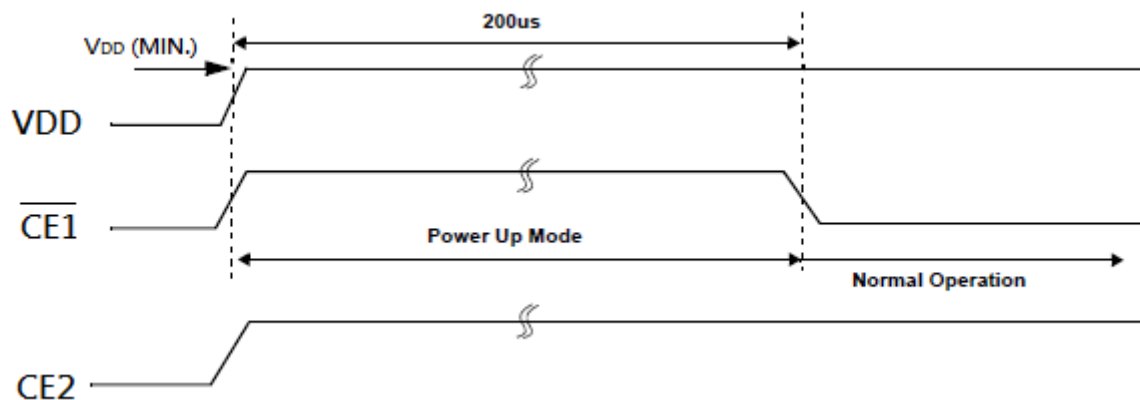
NOTES

1. AC measurement are assumed $t_R, t_F = 5\text{ns}$.
2. Parameters t_{HZ}, t_{OH}, t_{BHZ} and t_{WHZ} define the time at which the output goes the open condition and are not output voltage reference levels.
3. If $\overline{\text{OE}}$ is high during the write cycle, the outputs will remain at high impedance.
4. During the output state of DQ signals, input signals of reverse polarity must not be applied.
5. If $\overline{\text{CE1}}$ or $\overline{\text{LB}}/\overline{\text{UB}}$ goes LOW coincident with or after $\overline{\text{WE}}$ goes LOW, the outputs will remain at high impedance.
6. If $\overline{\text{CE1}}$ or $\overline{\text{LB}}/\overline{\text{UB}}$ goes HIGH coincident with or before $\overline{\text{WE}}$ goes HIGH, the outputs will remain at high impedance.

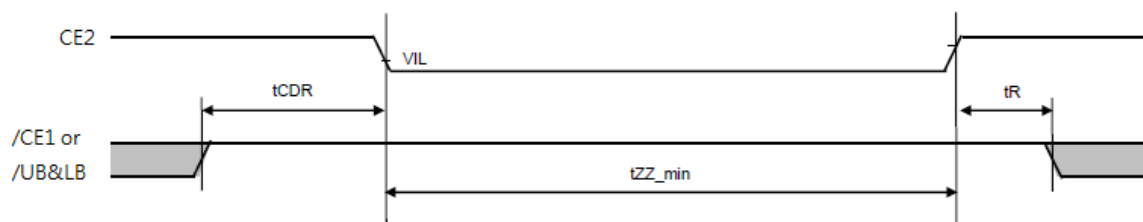
Page Read Cycle_16 Words Access



■ Power_On Timing

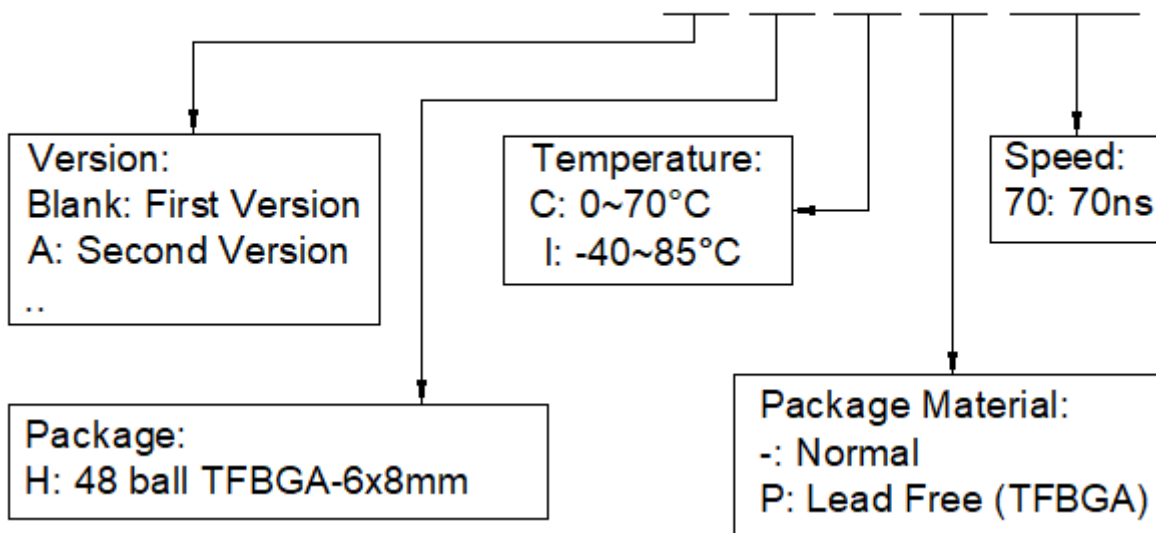


■ Deep Power Down Mode Entry/Exit



■ Order information

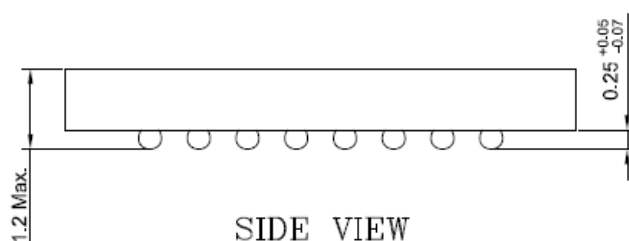
CS26LV32173X X X X XX



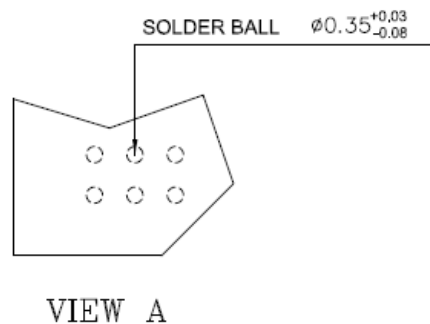
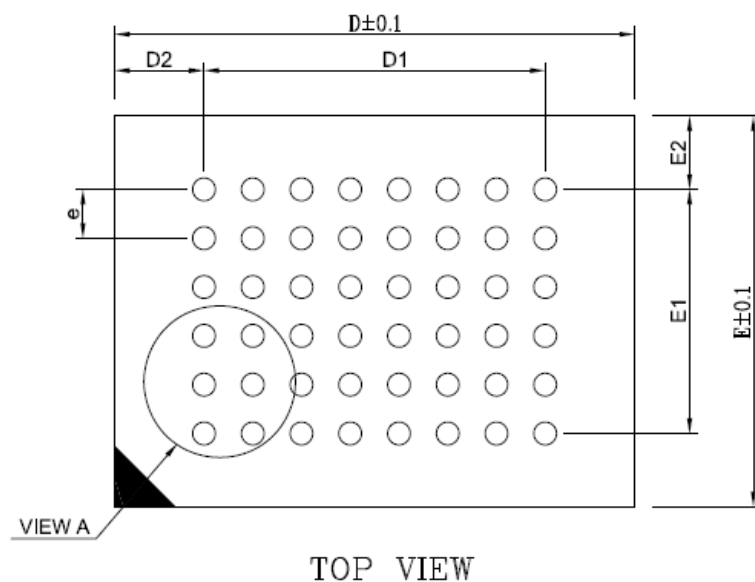
Note: Package material code "P" meets RoHS

■ Package Dimensions:

48 ball TFBGA-6x8mm



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
 LINEAR : X.X = ±0.1
 X.XX = ±0.05
 X.XXX = ±0.025