Revision History

Rev. No.	History	Issue Date
1.0	New issue	Oct. 05,2022

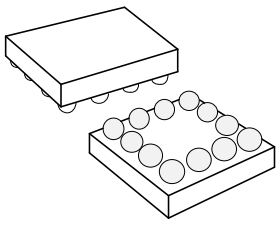
Dual-Channel Gate Driver for Enhancement Mode GaN FETs

Description

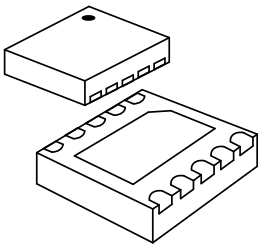
The CS8201 is a high performance dual gate driver optimized to drive half bridge N−Channel GaN FETs. A high floating top driver design can accommodate HB voltage as high as 80V. The CS8201 has split gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently.

In addition, the strong sink capability of the CS8201 maintains the gate in the low state, preventing unintended turn-on during switching. The CS8201 can operate up to several MHz. This device also supports supply input under voltage lockout.

The CS8201 uses 12 balls CSP package. and 10L DFN-3x3x0.75mm.



CSP(1.86x1.93x0.6mm)



DFN(3x3x0.75mm)

Features

- Independent High-Side and Low-Side TTL Logic Inputs
- 1.2A/5A Peak Source/Sink Current
- High-Side Floating Bias Voltage Rail Operates up to 80V_{DC}
- Split Outputs for Adjustable Turn-on/Turn-off Strength
- 0.6Ω /2.1Ω Pull-down/Pull-up Resistance
- Fast Propagation Times (30ns Typical)
- Excellent Propagation Delay Matching (1.5ns Typical)
- Supply Rail Under-Voltage Lockout
- Low Power Consumption

Applications

- Current Fed Push-Pull converters
- Half and Full-Bridge converters
- Synchronous Buck converters
- Two-switch Forward converters
- Forward with Active Clamp converters

Ordering & Marking Information

8201X

(1)Package Type

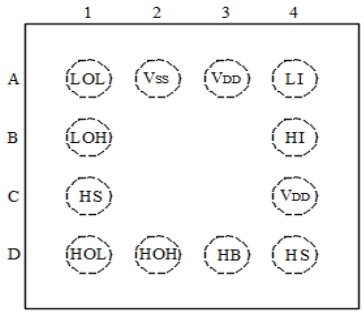
(2)Part Number

Package Type:

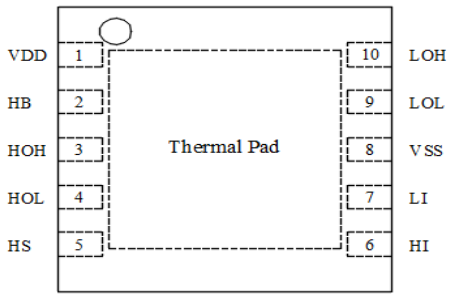
(1) M: 12 balls **CSP**

(2) Z: 10L DFN

Pin Configuration



12 balls CSP (Top View)

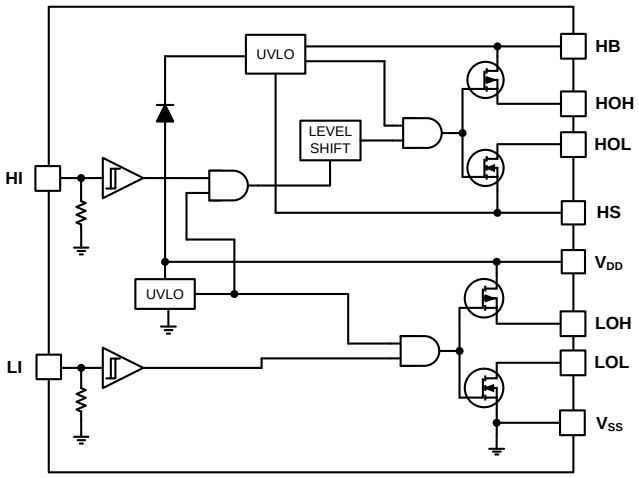


10L DFN (Top View)

Pin Description

PIN NO.	SYMBOL	DESCRIPTION
A3,C4	V_{DD}	Power Supply Pin
D3	HB	High−Side Bootstrap
D2	HOH	High-side gate driver turn-on output, use a resistor to set the turn-on speed.
D1	HOL	High-side gate driver turn-off output, use a resistor to set the turn-off speed.
C1,D4	HS	High-side source connection
B4	HI	High−Side Input
A4	LI	Low−Side Input
A2	V_{SS}	Ground
A1	LOL	Low-side gate driver sink-current output, use a resistor to set the turn-off speed.
B1	LOH	Low-side gate driver source- current output, use a resistor to set the turn-on speed.

Functional Block Diagram



■ Absolute Maximum Ratings (Note 1)

PARAMETER	RATINGS	UNIT
V_{DD} to V_{SS}	-0.3 ~ 7	V
HB to HS	-0.3 ~ 7	V
LI or HI Input	-0.3 ~ 7	V
LOH, LOL Output	-0.3 ~ V_{DD}+0.3	V
HOH, HOL Output	V_{HS}−0.3 ~ V_{HB}+0.3	V
HS to V_{SS}	−5V ~ +80	V
HB to V_{SS}	0 ~ 87	V
HB to V_{DD}	0 ~ 80	V
Junction Temperature	150	°C
Storage Temperature Range	−55 ~ +150	°C

■ Recommended Operation Conditions (Note 2)

PARAMETER	RATINGS	UNIT
V_{DD}	+4.5 ~ +5.5	V
LI or HI Input	0 ~ +5.5	V
HS	−5 ~ 80	V
HB	V_{HS} +4 ~ V_{HS} +5.5	V
HS Slew Rate	<50	V/ns
Junction Temperature	−40 ~ +125	°C

Note 1:Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device.
These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2:The device is not guaranteed to function outside its operating conditions.

■ Electrical Characteristics

Typical values represent the most likely parametric norm at T_A=25°C, and are provided for reference purposes only.
Unless otherwise specified, V_{DD}=V_{HB}=5V, V_{SS}=V_{HS}=0V, No Load on LOL and HOL or HOH and HOL.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
V_{DD} Quiescent Current	I_{DD}	LI=HI=0V, V_{DD}=V_{HB}=4V		0.08		mA
V_{DD} Operating Current	I_{DDO}	f=500kHz		1.8		mA
Total HB Quiescent Current	I_{HB}	LI=HI=0V		0.09		mA
Total HB Operating Current	I_{HBO}	f=500kHz		1.4		mA
HB to V_{SS} Current, Quiescent	I_{HBS}	HS=HB=80V		0.4		μA
HB to V_{SS} Current, Operating	I_{HBSO}	f=500kHz		0.35		mA
INPUT						
Input Voltage Threshold	V_{IR}	Rising Edge	1.85	2	2.15	V
Input Voltage Threshold	V_{IF}	Falling Edge	1.55	1.7	1.85	V
Input Voltage Hysteresis	V_{IHYS}			300		mV
Input Pulldown Resistance	R_I			200		kΩ
UNDER VOLTAGE PROTECTION						
V_{DD} rising threshold	V_{DDR}		3.2	3.8	4.5	V
V_{DD} threshold hysteresis	V_{DDH}			0.25		V
HB rising threshold	V_{HBR}		2.4	3.1	3.8	V
HB threshold hysteresis	V_{HBH}			0.25		V
LOW & HIGH SIDE GATE DRIVER						
Low-level output voltage	V_{OL}	I_{HOL}=I_{LOL}=100 mA		0.06		V
High-level output voltage V_{OH}=V_{DD}–LOH or V_{OH}=HB–HOH	V_{OH}	I_{HOH}=I_{LOH}=100 mA		0.2		V
Peak source current	I_{OHL}	HOH,LOH=0 V		1.2		A
Peak sink current	I_{OLL}	HOL,LOL=5 V		5		A
High-level output leakage current	I_{OHLK}	HOH,LOH=0 V		0.2	1.0	μA
Low-level output leakage current	I_{OLLK}	HOL,LOL=5 V		0.2	1.0	μA

Electrical Characteristics (continued)

Typical values represent the most likely parametric norm at T_A=25°C, and are provided for reference purposes only.
Unless otherwise specified, V_{DD}=V_{HB}=5V, V_{SS}=V_{HS}=0V, No Load on LOL and HOL or HOH and HOL.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
BOOTSTRAP DIODE AND CLAMP						
Low Current forward voltage	V_{DL}	I_{VDD-HB}=100μA		0.4		V
High Current forward voltage	V_{DH}	I_{VDD-HB}=50mA		0.9		V
Dynamic resistance	R_D	I_{VDD-HB}=50mA		1.85	3.6	Ω
HB-HS clamp regulation voltage	V_{CLAMP}		4.5	5	5.5	V

■ Switching Characteristics (over operating free-air temperature range)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LO turn-off propagation delay	t_{LPHL}	LI falling to LOL falling		30	45	ns
LO turn-on propagation delay	t_{LPLH}	LI rising to LOH rising		30	45	ns
HO turn-off propagation delay	t_{HPHL}	HI falling to HOL falling		30	45	ns
HO turn-on propagation delay	t_{HPLH}	HI rising to HOH rising		30	45	ns
Delay matching LO on & HO off	t_{MON}			1.5	8	ns
Delay matching LO off & HO on	t_{MOFF}			1.5	8	ns
HO rise time (0.5 V~4.5 V)	t_{HRC}	C_L=1000 pF		7		ns
LO rise time (0.5 V~4.5 V)	t_{LRC}	C_L=1000 pF		7		ns
HO fall time (0.5 V~4.5 V)	t_{HFC}	C_L=1000 pF		4		ns
LO fall time (0.5 V~4.5 V)	t_{LFC}	C_L=1000 pF		4		ns
Minimum input pulse width that changes the output	t_{PW}			10		ns

Detailed Operating Description

The CS8201 is designed to drive both the high-side and the low-side enhancement mode FETs in a synchronous buck or a half-bridge configuration. The CS8201 input has two separate HI and LI, the signaleach driving high side and Low side GaN FETs. HI logic high turns on the high-side gate driver and turns off the lowside gate driver. In reverse,LI logic high turns off the high side gate driver and turns onthe low side gate driver. If not used, it must be tied to the GND. These inputs must not be kept floating.

The CS8201 has an Under-voltage Lockout (UVLO) on both the V_{DD} and bootstrap supplies. When the V_{DD} voltage is below the threshold voltage of 3.8V, both the HI and LI inputs are ignored, to prevent the FETs from being partially turned on. Also if there is sufficient V_{DD} voltage, the UVLO will actively pull the LOL and HOL low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.1V, only HOL is pulled low.

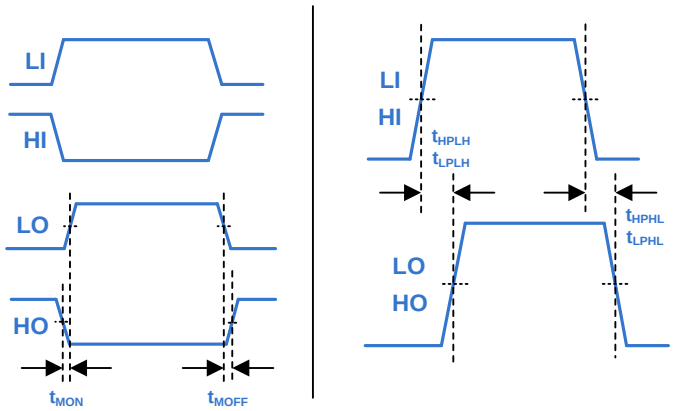
High-Side Driver

The high side driver uses the floating bootstrap capacitor voltage to drive the high-side FETs The bootstrap capacitor is recharged through an internal bootstrap diode each cycle when the HS pin is pulled below the V_{DD} voltage. For inductive load applications the HS node will fall to a negative potential, clamped by the low side FETs. Between HOH and HOL Pin, use a resistor(R_{HO}) to set the turn-on speed, the recommended resistance value is above 30Ω.

Low-Side Driver

The low-side driver is designed to drive a ground referenced FETs, The bias to the low-side driver s internally connected to V_{DD} supply and GND. Between LOH and LOL Pin, use a resistor(R_{LO}) to set the turn-on speed, the recommended resistance value is above 10Ω.

Timing Diagram

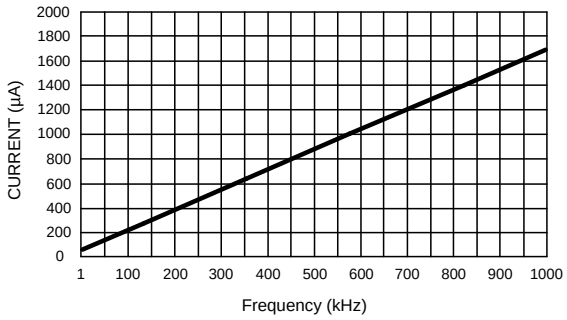


Truth Table

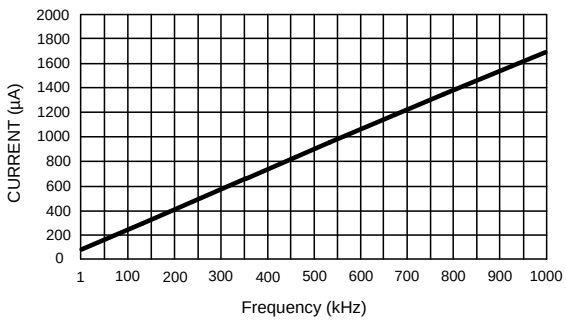
HI	LI	HOH	HOL	LOH	LOL
L	L	Open	L	Open	L
L	H	Open	L	H	Open
H	L	H	Open	Open	L
H	H	H	Open	H	Open

■ Typical Characteristics

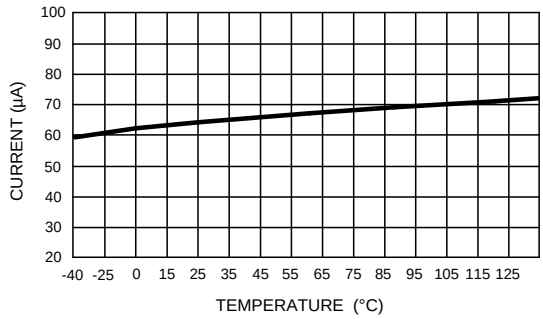
I_{DDO} vs Frequency



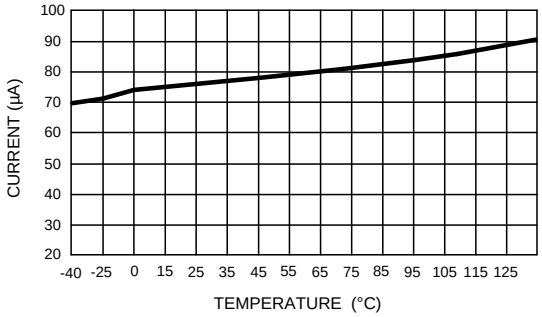
I_{HBO} vs Frequency



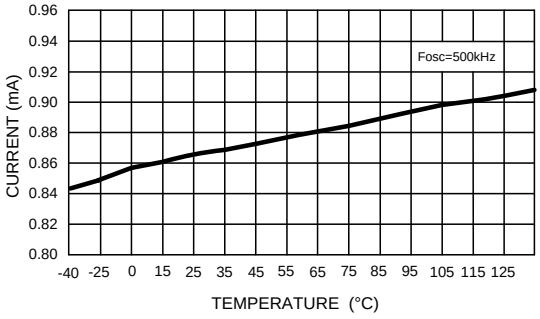
I_{DD} vs Temperature



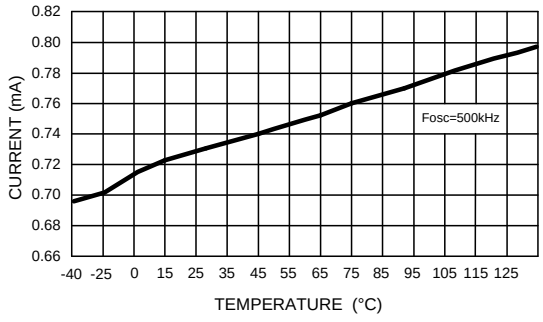
I_{HB} vs Temperature



I_{DD} vs Temperature

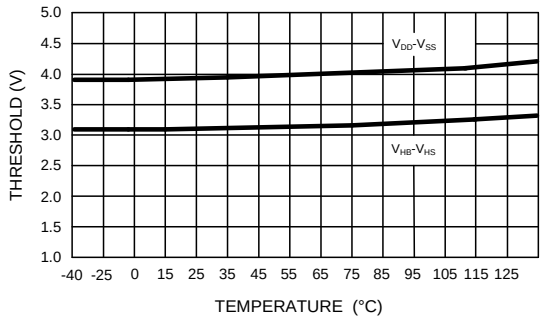


I_{HB} vs Temperature

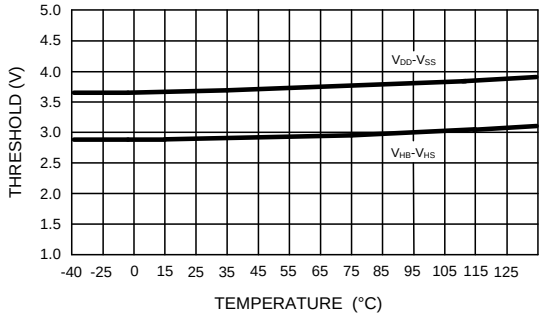


■ Typical Characteristics (continued)

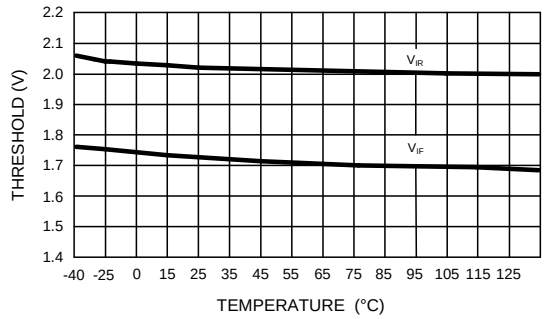
UVLO Rising Threshold vs Temperature



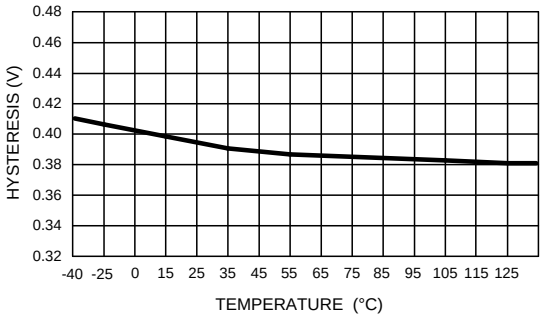
UVLO Falling Threshold vs Temperature



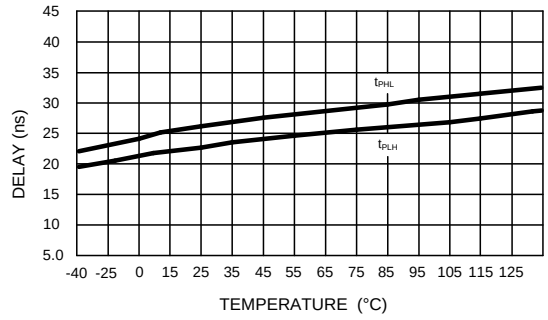
Input Threshold vs Temperature



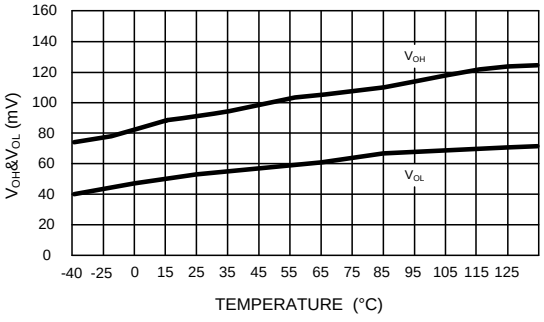
Input Threshold Hysteresis vs Temperature



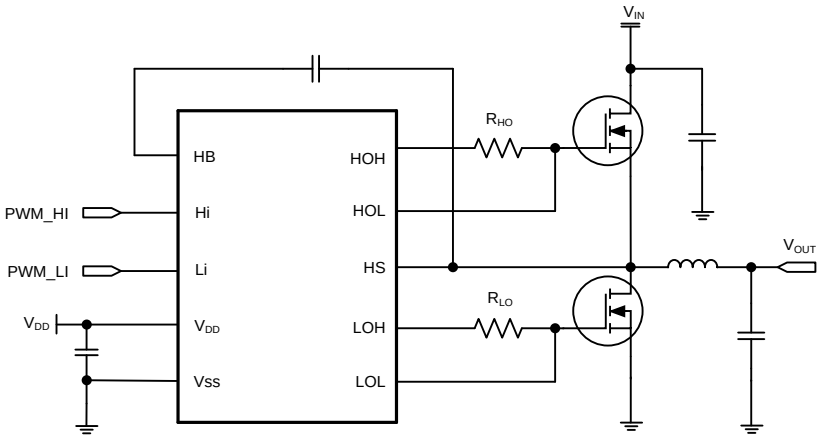
Propagation Delay vs Temperature



HO & LO Gate Drive vs Temperature



■ Typical Applications

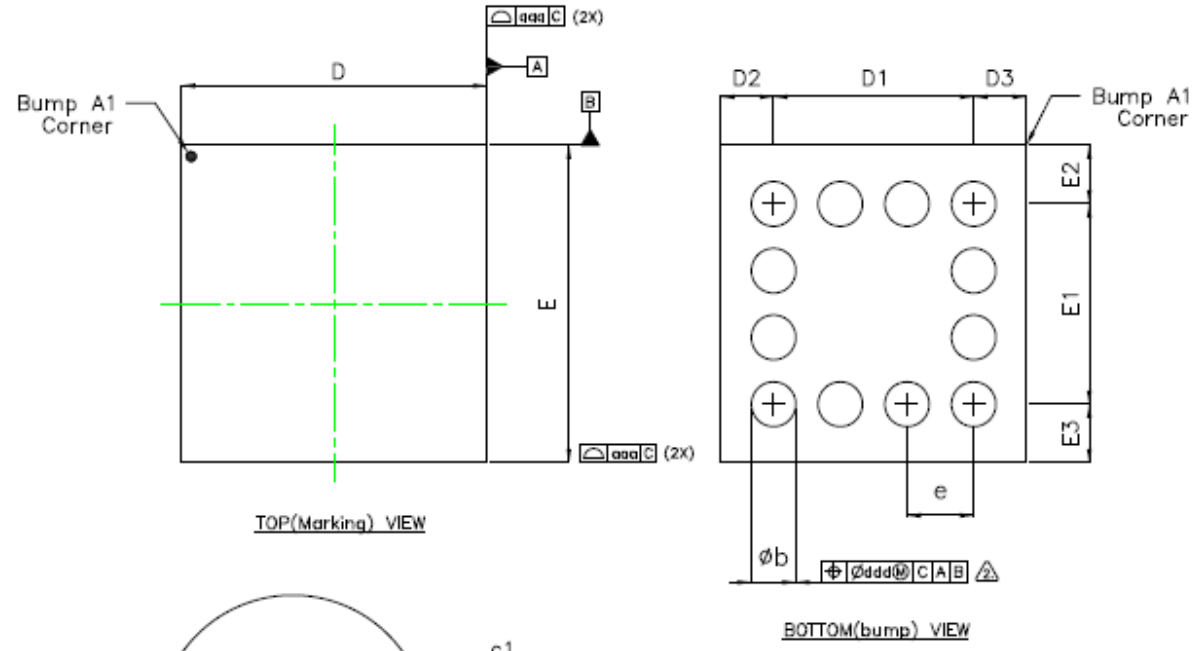


■ Layout Guidelines

Gate drivers experience high di/dt during the switching transitions. So, the inductance at the gate drive traces must be minimized to avoid excessive ringing on the switch node. Gate drive traces should be kept as short and wide as practical. The input capacitor must be placed as close as possible to the IC. Connect the V_{SS} pin of the CS8201 as close as possible to the source of the lower FETs. The use of vias is highly desirable to maximize thermal conduction away from driver.

■ Package outline

12 balls CSP with 1.86x1.93mm body size

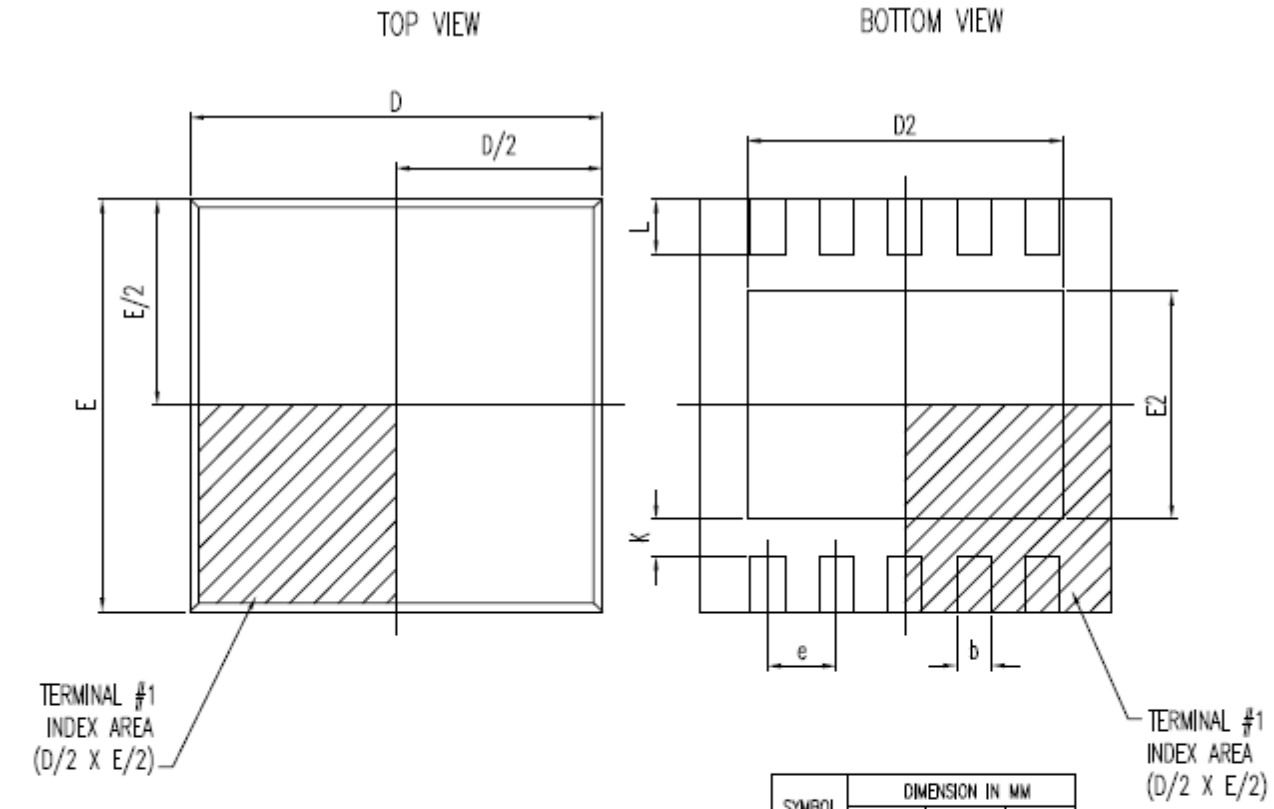


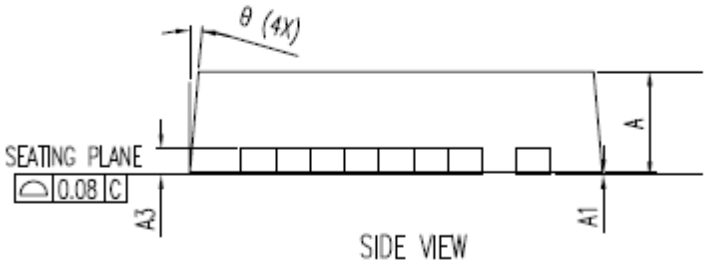
Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.5526	0.6000	0.6474	0.0218	0.0236	0.0255
A1	0.1746	0.1940	0.2134	0.0069	0.0076	0.0084
c1	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
c	0.3560	0.3810	0.4060	0.0140	0.0150	0.0160
D	1.8050	1.8325	1.8600	0.0711	0.0721	0.0732
E	1.8750	1.9025	1.9300	0.0738	0.0749	0.0760
b	0.2278	0.2680	0.3082	0.0090	0.0106	0.0121
D1	---	1.2000	---	---	0.0472	---
D2	---	0.3163	---	---	0.0125	---
D3	---	0.3163	---	---	0.0125	---
E1	---	1.2000	---	---	0.0472	---
E2	---	0.3513	---	---	0.0138	---
E3	---	0.3513	---	---	0.0138	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.0275	---	---	0.0011	---
bbb	---	0.0600	---	---	0.0024	---
ccc	---	0.0300	---	---	0.0012	---
ddd	---	0.0150	---	---	0.0006	---

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

10 L DFN-3x3x0.75mm





SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF.	
D		3.00 BASIC	
D2	2.20		2.70
E		3.00 BASIC	
E2	1.40		1.75
e		0.50 BASIC	
b	0.18	0.25	0.30
L	0.30	0.40	0.50
K	0.20		
θ	0°		14°
JEDEC	MO-229 (Variation W3030D-5)		